UNIVERSITÉ DU QUÉBEC À RIMOUSKI

LA CARACTÉRISATION DU TRANSISTOR PAR LE *TUNER SOURCE & LOAD PULL* POUR L'AMPLIFICATEUR DE PUISSANCE CLASSE F INVERSE

Mémoire présenté

dans le cadre du programme de maîtrise en ingénierie

en vue de l'obtention du grade de maîtrise ès sciences appliquées

PAR

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mars 2013

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Dépôt initial le 7 janvier 2013 Dépôt final le 27 mars 2013

REMERCIEMENTS

Je voudrais tout d'abord remercier mon professeur Chan-Wang Park qui, grâce à sa patience, sa passion et son professionnalisme, m'a non seulement guidé, orienté, conseillé et accompagné tout au long de ces trois années de recherches, mais également su me faire partager son expérience et me pousser à toujours me surpasser. Ainsi, si j'ai réussi à accomplir mon mémoire c'est en grande partie grâce à lui. Je tiens aussi à remercier toutes les personnes qui m'ont aidé dans la réalisation de mon travail et qui m'ont soutenue et encouragées ces dernières années. De plus, je tiens à remercier chaleureusement monsieur Karel Uhlir, Claude Bouchard et Traian Antonescu qui ont accepté de m'aider et m'ont grandement aidé en fabriquant les circuits imprimés me permettant de mener à bien ce projet. Je souhaiterai remercier les professeurs Mohammed Bahoura et Tayeb A. Denidni qui ont évalué mon mémoire, en me consacrant une part de leur temps précieux, et m'ont apporté des solutions de manière à améliorer mon travail. Finalement, je voudrai remercier tous mes collègues de l'Université du Québec à Rimouski et plus spécifiquement mes camarades du département de génie avec qui j'ai eu l'honneur de travailler et qui m'ont apporté leur aide, leurs expériences et leur soutien. Bien évidemment, je remercie infiniment ma famille pour son soutien moral qui m'a été extrêmement précieux afin de mener à bien ce projet.

RÉSUMÉ

Dans ce travail, la méthodologie de conception de premier passage pour des amplificateurs de puissance de classe F inverse est présentée. Pour concevoir l'amplificateur de puissance de classe F inverse à 3.5 GHz avec un signal 1-ton et un signal LTE, le transistor CGH40010 de Cree Inc. est analysé et caractérisé avec un signal 1-ton et un signal LTE. La caractérisation et l'analyse sont exploitées par la simulation *source & load pull* dans le logiciel ADS 2011.10 et par le système *source & load pull tuner* multi-harmonique passif de *Focus microwaves Inc.* Les $2^{ème}$ et $3^{ème}$ harmoniques à l'entrée et à la sortie du transistor sont pris en compte dans les caractérisations. L'analyse des résultats de la caractérisation par la simulation et par le système de *tuner* a prouvé que non seulement les $2^{ème}$ et $3^{ème}$ harmoniques à la sortie du transistor, mais également les $2^{ème}$ et $3^{ème}$ harmoniques à l'entrée du transistor sont importantes pour atteindre un rendement élevé et une puissance de sortie élevée. Le coefficient de réflexion (Γ) maximal du *tuner* passif à des fréquences harmoniques est important dans la caractérisation du transistor, car un Γ élevé peut augmenter le rendement en puissance ajoutée et la puissance de sortie de l'amplificateur de puissance de classe F inverse. Pour augmenter le coefficient de réflexion (Γ) maximal de *tuner*, les accessoires utilisés dans le système de *tuner*, tels que les circuits de polarisation, les coupleurs directifs et l'isolateur, sont analysés. Sur la base de cette analyse, le Γ maximal du *tuner* pourrait être augmenté de 0.902 à 0.930 par choisir les accessoires. Sur la base des résultats des caractérisations obtenus par la simulation et le système *source & load pull tuner*, les amplificateurs de classe F inverse sont conçus et fabriqués. En comparant les résultats mesurés des amplificateurs de puissance qui sont fabriqués sur la base des résultats de caractérisation correspondants obtenus par la simulation et le système de *tuner*, nous avons constaté que le système de *tuner* peut prédire les résultats, tel que le rendement en puissance ajoutée et la puissance de sortie, plus précisément que la simulation avec le modèle du transistor de grand signal. Pour l'amplificateur conçu sur la base des résultats de caractérisation obtenus par le système de *tuner* avec un signal 1-ton, lorsque la puissance de sortie est 40.02 dBm, le rendement en puissance ajoutée est 79.76% avec 12.08 dB de gain. Pour l'amplificateur conçu sur la base des résultats de caractérisation obtenus par le système de *tuner* avec un signal LTE, lorsque la puissance de sortie est de 34.20 dBm et le gain est 16.20 dB, le rendement en puissance ajoutée est 49.56%. Le taux de puissance du canal adjacent 1, qui a un décalage de 10 MHz, est -29.45 dBc, et le taux de puissance du canal adjacent 2, qui a un décalage de 20 MHz, est -50.87 dBc.

Mots clés : Le circuit de polarisation, la caractérisation de transistor, l'amplificateur de puissance de classe F inverse, *tuner source & load pull*.

ABSTRACT

In this work, a first-pass design methodology of designing the inverse class F power amplifier is presented. In order to design the inverse class F power amplifiers for the 1-tone signal and the LTE signal, Cree's CGH40010 transistor is analyzed and characterized with a 1-tone signal at 3.5 GHz and a LTE signal at 3.5 GHz with 10 MHz bandwidth. The characterization and analysis are operated by the source & load pull simulation in the software ADS 2011.10 with large signal transistor model and by the passive multi-harmonic source & load pull tuner system from Focus microwaves Inc. In the characterizations of transistor, 2^{nd} and 3^{rd} harmonic on both input and output side of the transistor are considered. The analysis of the transistor's characterization shows that, not only the 2^{nd} and 3^{rd} harmonics on the output side of the transistor are important to achieve high power added efficiency and output power for an inverse class F power amplifier, but also the 2^{nd} and 3^{rd} harmonics on the input side of the transistor. High reflection coefficient (Γ) achieved by the passive source and load pull tuner at harmonic frequencies is important in the transistor characterization, since the high Γ can increase the power added efficiency and the output power of the inverse class F power amplifier. To increase the maximum Γ of the passive tuner system, the accessories in the passive tuner system, such as bias tee, directional coupler and isolator, are analyzed. Based on the analysis, the maximum Γ of the passive tuner system could be increased from 0.902 to 0.930 by choosing the accessories. Based on the characterization results obtained by the simulation and the tuner system, bias circuit and impedance matching networks are analyzed and designed for the inverse class F power amplifiers. Bias circuit is designed to maximize the RF isolation to the DC input port and the return loss, and minimize the insertion loss at fundamental frequency. The inverse class F power amplifiers designed based on the characterization results are fabricated and measured. By comparing the measured results of the power amplifiers which fabricated based on the corresponding characterization results obtained by simulation and tuner system, we found that the multi-harmonic passive source & load pull tuner system can predict the power added efficiency and the output power more precisely than the simulation with the large signal transistor model. For the fabricated 1-tone inverse class F power amplifier designed based on the 1-tone characterization result obtained by the tuner system, when the output power is 40.02 dBm, the power added efficiency is 79.76% with a gain of 12.08 dB. For the fabricated LTE inverse class F power amplifier designed based on the LTE characterization result obtained by the tuner system, the measured output power is 34.20 dBm with a power added efficiency of 49.56% and a gain of 16.20 dB. The measured worst adjacent channel power ratio 1 with 10 MHz offset is -29.45 dBc. The measured worst adjacent channel power ratio 2 with 20 MHz offset is -50.87 dBc.

Keywords : Bias circuit, characterization, inverse class F power amplifier, source & load pull tuner.

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3G	*3rd Generation.*
	3ème Génération.
4G	*4th Generation.*
	4ème Génération.
5G	*5th Generation.*
	5ème Génération.
ACPR	*Adjacent Channel Power Ratio.*
	Taux de Puissance du Canal Adjacent.
ADS	*Advanced Design System.*
	Conception des Systèmes Avancés.
DC	*Direct Current.*
	Courant Continu.
DPD	*Digital Predistortion.*
	Prédistorsion Numérique.
DUT	*Device Under Test.*
	Dispositif Sous Essai.

EM	*Electromagnetic.*
	Électromagnétique.
E-TM	*E-UTRA Test Model.*
	Modèle de Test pour E-UTRA.
E-UTAR	*Evolved Universal Terrestrial Access.*
	Accès Terrestre Évolué Universel.
FET	*Field Effect Transistor.*
	Transistor à Effet de Champ.
GaAs	*Gallium Arsenide.*
	L'Arséniure de Gallium.
GaN	*Gallium Nitride.*
	Nitrure de Gallium.
GPIB	*General Purpose Interface Bus.*
	Bus d'Interface Général.
HEMT	*High Electron Mobility Transistor.*
	Transistor à Haute Mobilité d'Électrons.
HSPA	*High Speed Packet data Access.*
	Haute Vitesse par Paquets de Données d'Accès.
LSNA	*Large Signal Network Analyzer.*
	L'analyseur de Réseau de Grand Signal.

LTE	*Long Term Evolution.*
	Évolution à Long Terme.
MIMO	*Multiple Input Multiple Output*
	Entrées Multiples et Sorties Multiples
PA	*Power Amplifier.*
	Amplificateur de Puissance.
PAE	*Power Added Efficiency.*
	Rendement en Puissance Ajoutée.
TDD	*Time Division Duplex.*
	Duplexage par Répartition Temporelle.
VNA	*Vector Network Analyzer.*
	L'analyseur de Réseau Vectorielle.
W-CDMA	*Wideband Code Division Multiple Access.*
	Large bande d'Accès Multiple par Répartition en Code.

CHAPITRE 1
INTRODUCTION GÉNÉRALE

1.1 PROBLÉMATIQUE

L'amplificateur de puissance (AP) à haute efficacité n'est pas encore fabriqué à grande échelle en raison de l'absence de la méthodologie de conception de premier passage qui nous permet d'avoir de bons résultats lors de la première fabrication. La méthodologie de conception de premier passage signifie que le produit fabriqué fonctionne comme prévu, sans la postproduction. Les conceptions d'un AP pratique sont souvent empiriques, où l'expérience et le réglage de la postproduction sont utilisés pour obtenir les résultats souhaités de l'amplificateur. Cependant, cette méthode ne peut pas être utilisée pour une fabrication à grande échelle dans l'industrie des APs, en raison du réglage coûteux de postproduction. Les réglages postproductions peuvent inclure l'ajustement de la tension pour les APs, tel que V_{GS} et V_{DS}, ou l'ajustement de la longueur des *stubs* dans les circuits des APs en les coupant. La méthodologie de conception de premier passage pourrait aider l'industrie à fabriquer des AP d'une haute efficacité à grande échelle sans le réglage de la postproduction. (Wu *et al.*, 2010a). Dans ce mémoire, une méthodologie de conception de premier passage pour concevoir un AP de classe F inverse pour un signal 1-ton et un signal évolution à long terme (LTE) va être développée. Lors de la réalisation de cette idée, certaines problématiques ont été rencontrées. Les problématiques sont divisées en cinq sous-sections. Elle sont présentées, respectivement, les problématiques associées aux éléments suivants: l'AP pour le signal LTE, l'AP de classe F inverse, la caractérisation par le *tuner source & load pull* multi-harmonique, l'effet des $2^{ème}$ et $3^{ème}$ harmoniques de la source de l'amplificateur, et le Γ maximal du *tuner source & load pull* passif.

Dans la première sous-section de l'AP pour le signal LTE (sous-section 1.1.1), pour obtenir un design de premier passage d'un AP pour le signal LTE, le signal LTE et l'état de l'art des APs conçus par d'autres auteurs pour le signal LTE sont étudiés. Ces APs sont réalisés sur la base de la caractérisation du modèle de transistor de grand signal. Cependant, les travaux publiés indiquent que le modèle du transistor de grand signal parfois n'est pas assez précis. Ainsi, dans cette section, la question est de savoir comment on pourrait caractériser le transistor assez précisément pour parvenir à une conception de premier passage pour l'AP.

Dans la seconde sous-section d'un AP de classe F inverse (sous-section 1.1.2), afin de concevoir un AP de classe F inverse, la conception de base de l'AP de classe F inverse et l'état de l'art des APs de classe F inverse conçus par d'autres auteurs sont étudiés. Pour obtenir une efficacité élevée dans un AP de classe F inverse, théoriquement, tous les harmoniques sur le côté de la sortie du transistor (les harmoniques de la charge) doivent être contrôlées. Toutefois, il est impossible de contrôler tous les harmoniques, de sorte que la question de cette section est de savoir combien d'harmoniques doivent être contrôlés pour avoir une efficacité suffisante?

En étudiant les APs de classe F inverse conçues par d'autres auteurs, nous avons trouvé que les $2^{ème}$ et $3^{ème}$ harmoniques sur le côté d'entrée du transistor (les $2^{ème}$ et $3^{ème}$ harmoniques de la source) sont également importantes pour atteindre une puissance de sortie et un rendement en puissance ajoutée (PAE) élevés. Puissance de sortie est la puissance mesurée à la sortie de l'AP. Le rendement en puissance ajoutée est définie comme ci-dessous (Kazimierczuk, 2008 : 6):

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \times 100\% \qquad (1)$$

où P_{out} est la puissance de sortie d'AP. P_{in} est la puissance d'entrée d'AP. P_{DC} est la puissance de courant continu ajoutée à l'AP. Pour concevoir un AP de classe F inverse à haute efficacité, les effets des $2^{ème}$ et $3^{ème}$ harmoniques de la source doivent être analysés

pour améliorer le PAE et la puissance de sortie de l'AP de classe F inverse. Ainsi, dans la troisième sous-section 1.1.3 pour les $2^{ème}$ et $3^{ème}$ harmoniques de la source, la question est de savoir comment les $2^{ème}$ et $3^{ème}$ harmoniques de la source affectent l'efficacité des APs de classe F inverse?

Pour réaliser une conception de premier passage d'un AP de classe F inverse et analyser l'effet $2^{ème}$ et $3^{ème}$ harmoniques à la fois sur le côté d'entrée et sur le côté de sortie du transistor, le système *source & load pull tuner* multi-harmonique est recommandé. Dans la quatrième sous-section du système *source & load pull tuner* multi-harmonique, la conception de base du système *source & load pull tuner* et l'état de l'art des APs conçus par le système *source & load pull tuner* sont étudiés. Cependant, les recherches réalisées par un autre auteur n'ont pas considéré les $2^{ème}$ et $3^{ème}$ harmoniques de la charge. Sur la base de la discussion dans la sous-section 1.1.3, les $2^{ème}$ et $3^{ème}$ harmoniques de la source doivent également être prises en considération, de sorte que la question de sous-section 1.1.4 est de savoir comment caractériser le transistor par le système *source & load pull tuner* multi-harmonique en considérant les $2^{ème}$ et $3^{ème}$ harmoniques de la source et la charge?

Basé sur la recherche de (Wu *et al.*, 2010b), le coefficient de réflexion (Γ) d'entrée et de sortie du transistor à des fréquences harmoniques devrait être proche de 1 pour atteindre une haute efficacité pour les APs de classe F inverse. Le Γ est le rapport de l'amplitude de l'onde réfléchie à l'amplitude de l'onde incidente. Quand il est égal à 1 à la fréquence harmonique, le signal à la fréquence harmonique peut être réfléchi et l'efficacité pour les APs de classe F inverse peut être augmentée. Par conséquent, dans sous-section 1.1.5, la question est de savoir comment augmenter le Γ maximal du système *source & load pull tuner*?

1.1.1 L'AP pour le signal LTE

La 3ème génération (3G) des normes de communication sans fil, telles que l'accès multiple par répartition de code large bande (W-CDMA), haute vitesse par paquets de données d'accès (HSPA) et HSPA+, peut offrir un débit maximal de 42 Mbps (3GPP org., 2012a). Aujourd'hui, avec le progrès de la technologie des télécommunications, la 4ème génération (4G) des normes de communication sans fil, telles que LTE et LTE-Avancé, pourrait fournir un plus haut débit et une meilleure qualité de service. LTE est développé pour de nombreuses bandes de fréquences, allant de 800 MHz à 3.5 GHz. Les largeurs de bande prises en charge sont de 1.4 MHz à 20 MHz. Avec une bande passante de transmission à 20 MHz et une architecture à entrées multiples et sorties multiples 4x4 (MIMO) dans la liaison descendante, le débit maximal théorique est 300 Mbps (3GPP org., 2012b). LTE-Avancé, comme une évolution de la technologie LTE, prend en charge jusqu'à 100 MHz de bande passante (3GPP org., 2012c). Un taux de données entrantes de 1 Gbps pourrait être réalisé par un système 4x4 MIMO et une bande passante de transmission de 70 MHz (3GPP org., 2009).

Pour concevoir un AP qui satisfait les exigences de LTE ou LTE-Avancé, une caractérisation du transistor à grand signal est essentielle pour estimer la puissance de sortie, le gain, le PAE et le rapport de puissance adjacente de canal (ACPR) dans le domaine non linéaire. L'ACPR est le ratio de la puissance moyenne dans le canal adjacent de fréquence (ou décalage) à la puissance moyenne dans le canal de fréquence transmise. Le modèle du transistor de grand signal est souvent utilisé pour concevoir des APs dans le simulateur comme *Advanced Design System* (ADS) (Wang *et al.*, 2011; Wang *et al.*, 2012a; Kim *et al.*, 2009).

Dans les travaux de recherches publiés par d'auteurs différents, l'AP LTE est généralement conçu avec le modèle du transistor de grand signal. Dans le travail (Moon *et al.*, 2011), un AP avec le transistor CGH40010 de Cree Inc. est présenté. L'AP est conçu sur la base de la caractérisation par simulation avec le modèle du transistor de grand signal.

L'AP fabriqué sans prédistorsion numérique (DPD) pourrait offrir 29.05% de PAE lorsque la puissance de sortie est 34.99 dBm, le gain est 13.29 dB. L'ACPR 1, qui a un décalage de 7.5 MHz, est -25.14 dBc, et l'ACPR 2, qui a un décalage de 12.5 MHz, est -32.24 dBc sous excitation du signal LTE à 1.84 GHz avec 10 MHz de bande passante. Avec une linéarisation par DPD, les ACPRs avec 7.5 et 12.5 MHz de décalage sont améliorés à -45.20 et -46.00 dBc, respectivement. Alors, le PAE est 32.16% à 34.72 dBm de puissance de sortie et 10.62 dB de gain. Les recherches sur la linéarisation par DPD (Draxler *et al.*, 2006; Kimball *et al.*, 2008; Cité par Kim *et al.*, 2010a) montrent qu'avec la technologie de linéarisation par DPD, l'ACPR a pu être améliorée de 21-22 dBc.

Dans (Kim *et al.*, 2010b), un AP multi-bande avec la $2^{ème}$ harmonique contrôlée est présenté. L'AP multi-bande est conçu sur la base des résultats de caractérisation avec un signal 1-ton par simulation avec le modèle du transistor de grand signal de transistor CGH40015 à 1.85 GHz, 1.96 GHz et 2.14 GHz. Avec un signal LTE à 2.14 GHz ayant une bande passante de 10 MHz, le PAE d'AP est 34.40% à la puissance de sortie de 36.10 dBm avec -29.40 dBc de pire ACPR sans linéarisation par DPD. Le décalage d'ACPR n'est pas indiqué dans l'article. Avec une linéarisation par DPD, la pire ACPR est améliorée à -55.00 dBc.

Dans (Markos *et al.*, 2010), un AP asymétrique Doherty de 50W est réalisé pour fonctionner à 2.50 GHz. L'AP est conçu sur la base des résultats de caractérisation 1-ton obtenus par simulation avec le modèle du transistor de grand signal. Avec un signal LTE de 10 MHz de bande passante, le PAE d'AP est de 43.00% à 40.00 dBm de puissance de sortie lorsque l'ACPR est -35.00 dBc avant la linéarisation par DPD (-46 dBc après la linéarisation).

Comme mentionné précédemment, les modèles de transistor grand signal sont généralement utilisés pour concevoir des APs. Cependant, les autres auteurs (Jung *et al.*, 2009; Liu *et al.*, 2003; De Groote *et al.*, 2007) montrent que le modèle du transistor de grand signal n'est parfois pas assez précis. Ainsi, la question est de savoir comment nous

pouvons caractériser avec précision le transistor avec un signal LTE afin que nous puissions concevoir un AP de classe F inverse pour un signal LTE.

1.1.2 L'AP de classe F inverse

L'AP de classe F inverse est habituellement employé pour atteindre une PAE de niveau élevé. Selon (Grebennikov, 2005 : 265; Saad *et al.*, 2009), une efficacité de 100% peut être obtenue en théorie, si toutes les harmoniques de charge sont contrôlées,. Idéalement, pour un AP de classe F inverse, toutes les harmoniques paires doivent être court-circuitées et les harmoniques impaires doit être en circuit ouvert. La forme d'onde du courant et la forme d'onde de la tension du transistor sont respectivement carrées et demi-sinusoïde, comme les montres dans Figure 1 (Grebennikov *et al.*, 2007). Cela signifie que la perte de puissance due au dispositif de connexion peut être réduite au minimum, car les résultats de l'intégration donnera une valeur faible par rapport à la puissance fournie à la charge sur la période où le courant minimal est correspond à la tension maximale (Kazimierczuk, 2008 : 267).

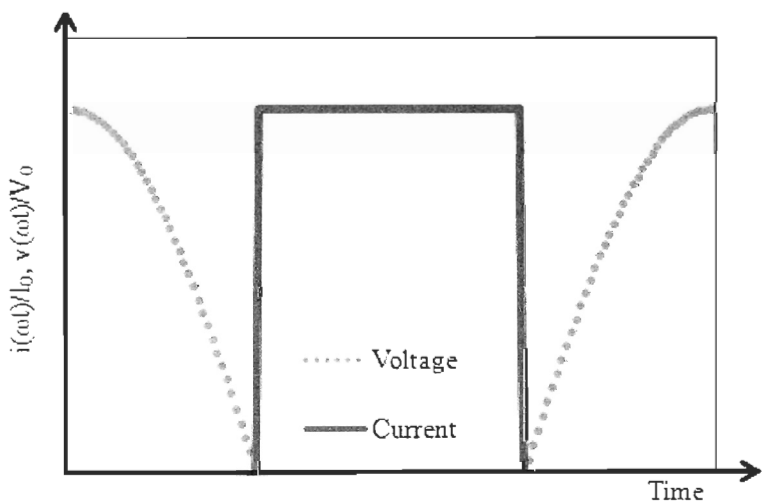


Figure 1 : La tension (ligne pointillée) et le courant (ligne continue) normalisés des formes d'onde d'un AP idéal de classe F inverse avec toutes les harmoniques contrôlées

Les formes d'onde de la Figure 1 peuvent être exprimées sous la forme de séries de Fourier, comme aux équations (2) et (3) (Helaoui *et al.*, 2009). Les variables *i(ωt)* et *v(ωt)* sont de forme d'onde de courant carrée et de forme d'onde de tension demi-sinusoïdale, respectivement. ω est la fréquence angulaire et I_0 et V_0 sont les composantes de courant continu et de tension. Le Tableau 1 montre l'efficacité obtenue lorsque différentes composantes harmoniques de tension et de courant sont contrôlées. Pour plus d'efficacité, plus d'harmoniques doivent être contrôlées.

$$\frac{\mathrm{i}(\omega t)}{\mathrm{I}_0} = 1 + \frac{4}{\pi}\sin(\omega t) + \frac{4}{\pi}\sum_{n=3,5,7,\ldots}^{N}\frac{\sin(n\omega t)}{n} \tag{2}$$

$$\frac{\mathrm{v}(\omega t)}{\mathrm{V}_0} = 1 - \frac{\pi}{2}\sin(\omega t) - 2\sum_{n=2,4,6,\ldots}^{N}\frac{\cos(n\omega t)}{n^2-1} \tag{3}$$

Table 1 : Efficacité de différentes combinaisons de tension et de courant composantes harmoniques

Composantes harmoniques de courant	**Composantes harmoniques de tension**			
	1	1, 3	1, 3, 5	1, 3, 5, …, ∞
1	0.5	0.56	0.59	0.64
1, 2	0.67	0.75	0.78	0.85
1, 2, 4	0.71	0.80	0.83	0.91
1, 2, 4,…, ∞	0.79	0.88	0.92	1

Toutefois, il est impossible de contrôler toutes les fréquences harmoniques (Xu *et al.*, 2010; Aflaki *et al.*, 2008). Selon (Negra *et al.*, 2007; Raab, 1997), les deux premières harmoniques de charge (harmoniques $2^{ème}$ et $3^{ème}$) sont les harmoniques les plus importantes pour atteindre une efficacité élevée pour des APs. Les formes d'ondes de tension et de courant lorsque seules les $2^{ème}$ et $3^{ème}$ harmoniques sont contrôlées sont représentées sur la Figure 2 (Ebrahimi *et al.*, 2009).

Dans (Raab, 1997; Grebennikov, 2005 : 257), théoriquement, 75% d'efficacité pourrait être atteint si les deux premières harmoniques étaient correctement terminées à la sortie du transistor. Ainsi, dans le but de concevoir un AP de classe F inverse, les 2ème et 3ème harmoniques à la sortie du transistor doivent être prises en compte dans la caractérisation du transistor.

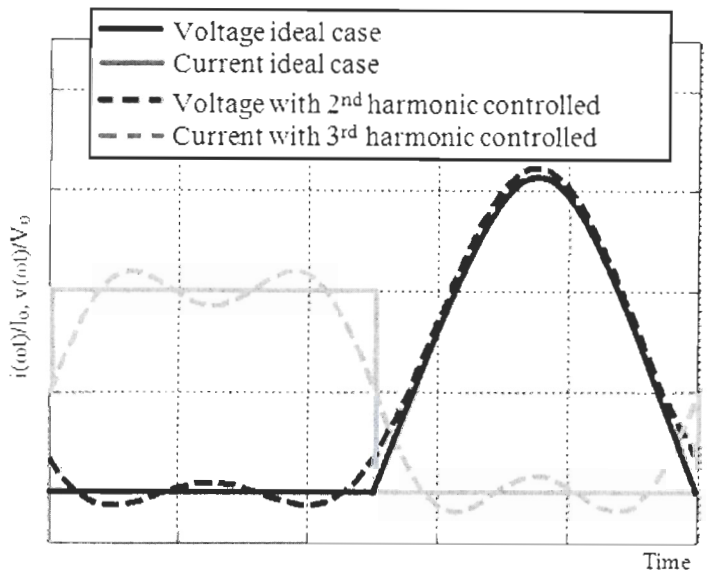


Figure 2 : Formes d'onde de la tension (noir) et le courant (gris) d'un AP de classe F inverse idéal avec toutes les harmoniques contrôlées (ligne continuée) et avec les 2ème et 3ème harmoniques contrôlées (ligne pointillée)

1.1.3 La caractérisation par le *tuner source & load pull* multi-harmonique passive

Pour concevoir un AP de classe F inverse, le *tuner source & load pull* est recommandé pour la caractérisation à grand signal d'un transistor (Colantonio *et al.*, 2009). Il existe deux technologies de système *source & load pull tuner*: actif et passif. Le système *load pull tuner* actif peut régler l'impédance de source/charge (ou facteur de réflexion) au plan de référence du dispositif sous essai (DUT) en utilisant une charge virtuelle: une partie

du signal sortant est modifié en amplitude et en phase par un réseau d'amplificateur/déphaseur et réinjecté à la sortie du transistor. Le coefficient de réflexion (Γ) au plan de référence du transistor peut être égal à 1, en raison de l'amplification. L'avantage de *tuner* actif est qu'il permet d'avoir une Γ plus haute (supérieur à 1). Cependant, des oscillations peuvent se produire, puisque le transistor fait partie de la boucle active (Focus microwaves Inc., 2012a).

Afin de protéger les transistors dû à l'oscillation indésirable, les tuners passifs sont recommandés. Le *tuner source/load pull* passif, comme le montre la Figure 3, peut régler l'impédance de source/charge au plan de référence du *DUT* en modifiant la position des sondes sans oscillation. Un autre avantage du *tuner* passif, c'est qu'il a une plus grande capacité de traitement de puissance par rapport au *tuner* actif (Ghannouchi *et al.*, 2010).

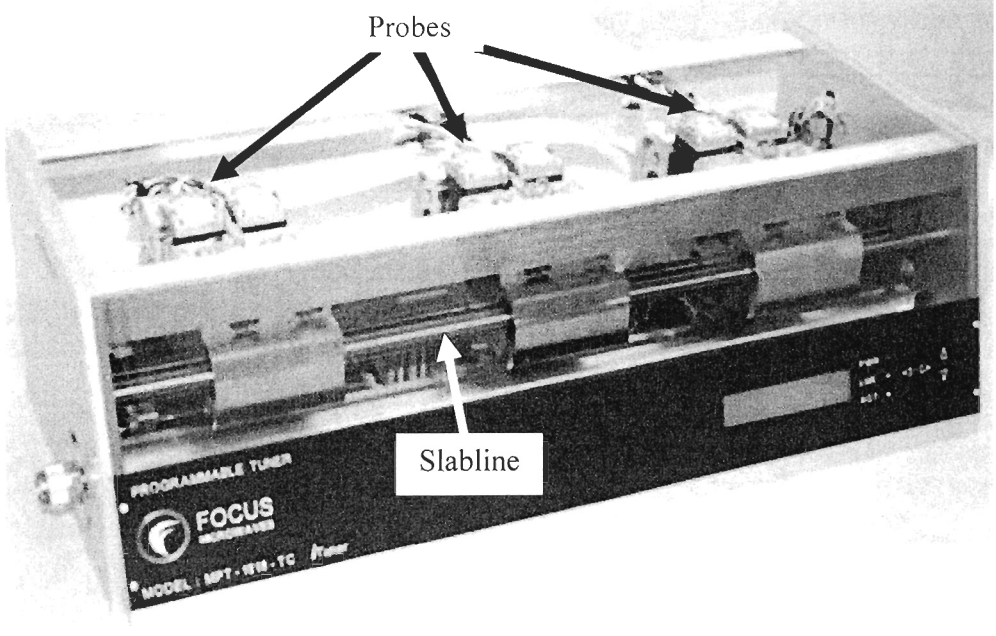


Figure 3 : Le *tuner source/load pull* passif

Les *source/load pull tuners* multi-harmoniques passifs peuvent régler l'impédance de source/charge à la fondamentale, $2^{ème}$ et $3^{ème}$ harmonique en même temps au plan de référence du *DUT*. Dans le *tuner* passif multi-harmonique représenté sur la Figure 3, il y a

3 sondes qui peuvent être déplacées verticalement et horizontalement le long de la *slabline* pour trois fréquences différentes. Comme le montre la Figure 4, lorsque la sonde est descendue dans la *slabline* (direction Y), elle interrompt le champ électrique et crée une capacité, augmentant ainsi l'ampleur de l'impédance. Lorsque la sonde se déplace le long de la *slabline* (direction X), la phase de l'impédance est mise en rotation. Un algorithme dans le logiciel de commande des *tuners* est utilisé pour déterminer le positionnement correct de chaque sonde pour les impédances désirées aux fréquences fondamentales et harmoniques (Focus microwaves Inc., 2012a; Maury microwave Inc., 2009).

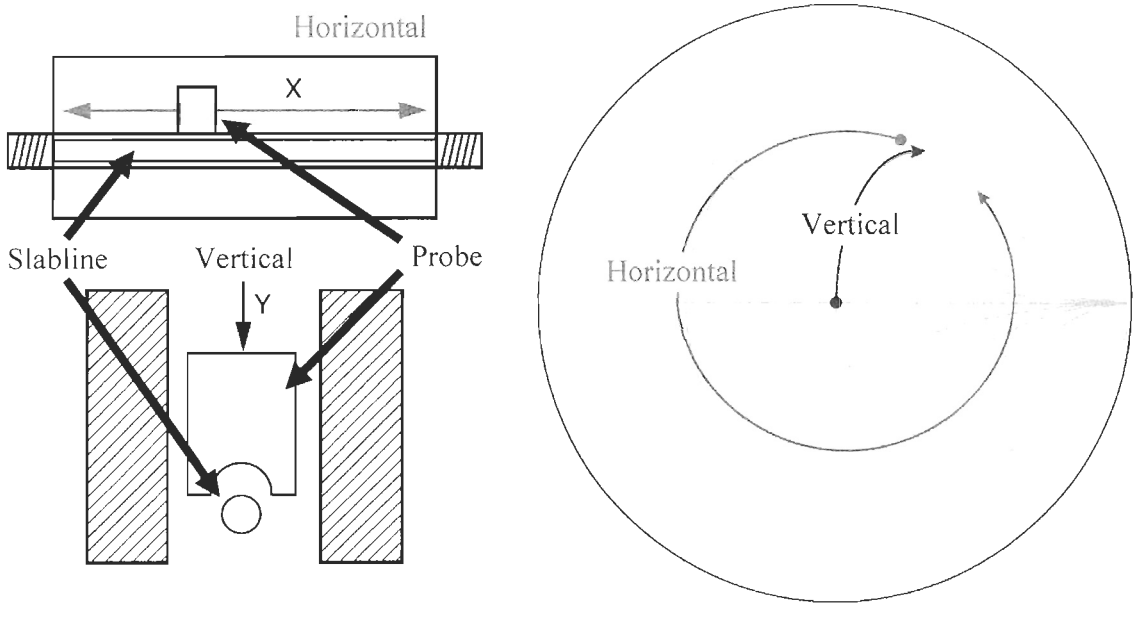


Figure 4 : Mécanisme du *source/load pull tuner* passif (Maury microwave Inc., 2009)

Les recherches antérieures (De Groote *et al.*, 2007; Ghannouchi *et al.*, 2009; Deshours *et al.*, 1997; Ghannouchi *et al.*, 1994) montrent que le transistor peut être caractérisé précisément pour le signal 1-ton et le signal 2-ton à l'aide du système *source & load pull tuner* passif.

Dans (Ghannouchi *et al.*, 1994), les système *source & load pull tuners* pour fréquence fondamentale sont utilisés pour caractériser un transistor gallium arséniure à effet

de champ (GaAs FET) avec un signal 1-ton (2.70 GHz) et un signal 2-ton (2.700 GHz et 2.695 GHz). L'objectif de ce travail est de comparer les résultats de la caractérisation 1-ton et 2-ton pour déterminer quelle méthode est la plus appropriée pour l'AP utilisé dans les systèmes de communications multi-porteuses. Dans leur analyse, la caractérisation par le *tuner source & load pull* pour un signal 2-ton est plus approprié pour caractériser la non-linéarité, la capacité de puissance et l'efficacité des amplificateurs pour utilisation dans les systèmes de communication multi porteuses.

Dans (Ghannouchi *et al.*, 2009), un *tuner source pull* de 1-ton, un *tuner load pull* de 1-ton et un *tuner* harmonique sont utilisées pour caractériser le transistor CGH40010 à 2.45 GHz. La caractérisation est actionnée lorsque la puissance d'entrée est de 25.00 dBm. Les résultats montrent que dans la caractérisation, une PAE de 75.95% peut être obtenue avec une puissance de sortie de 39.55 dBm. Sur la base des résultats de caractérisation, un AP de classe F inverse est fabriqué. Les résultats de la mesure montrent qu'il délivre une puissance de sortie de 39.40 dBm avec une PAE de 71.20%.

Dans (De Groote *et al.*, 2007), le système *load pull tuner* multi-harmonique de *Focus microwaves Inc.* et le système d'analyse de réseau de grand signal (LSNA) dans le domaine temporel sont utilisés pour effectuer la caractérisation d'un transistor à haute mobilité d'électrons (HEMT) nitrure de gallium (GaN) à 2.40 GHz. Les résultats montrent qu'une PAE de 59.70% peut être obtenue lorsque la puissance de sortie est de 35.40 dBm et le gain est de 21.40 dB.

Le tableau 2 résume les résultats des recherches présentés dans cette section. On y retrouve les résultats de caractérisation des transistors avec des *tuners source & load pull*. Dans les travaux présentés, la caractérisation ne considère que les $2^{ème}$ et $3^{ème}$ harmoniques dans les charges.

Table 2 : List des travaux présentés de la caractérisation par le système *source & load pull tuner*

Références	Fréquence contrôlée par le *tuner source pull*	Fréquences contrôlées par le *tuner load pull*	Transistor	Fréquence (GHz)	P_{out} (dBm)	PAE (%)
(De Groote *et al.*, 2007)	f_0	f_0, $2f_0$, $3f_0$	GaN HEMT	2.40	35.40	59.70
(Ghannouchi *et al.*, 2009)	f_0	f_0, $2f_0$, $3f_0$	CGH40010	2.45	39.55	75.95
(Fennelly et al., 1997)	f0	f0, 2f0, 3f0	Fujitsu FLL101 FET	CDMA @ 0.9 (1.23MHz BW)	25.0	44.1

1.1.4 Les 2ème et 3ème harmoniques de la source

Pour les harmoniques de la source, selon (Gao et al, 2006; cité par Wu et al, 2010b), le PAE est également sensible à l'impédance de source aux 2ème et 3ème harmoniques. Le PAE pourrait être réduite jusqu'à 15% lorsque la phase de l'impédance de source à la 2ème harmonique change de 10°, comme indiqué sur la Figure 5 (Wu *et al.*, 2010a). Ainsi, afin de concevoir un AP de classe F inverse, les 2ème et 3ème harmoniques de la source et de la charge doivent être pris en considération pour la caractérisation de un transistor.

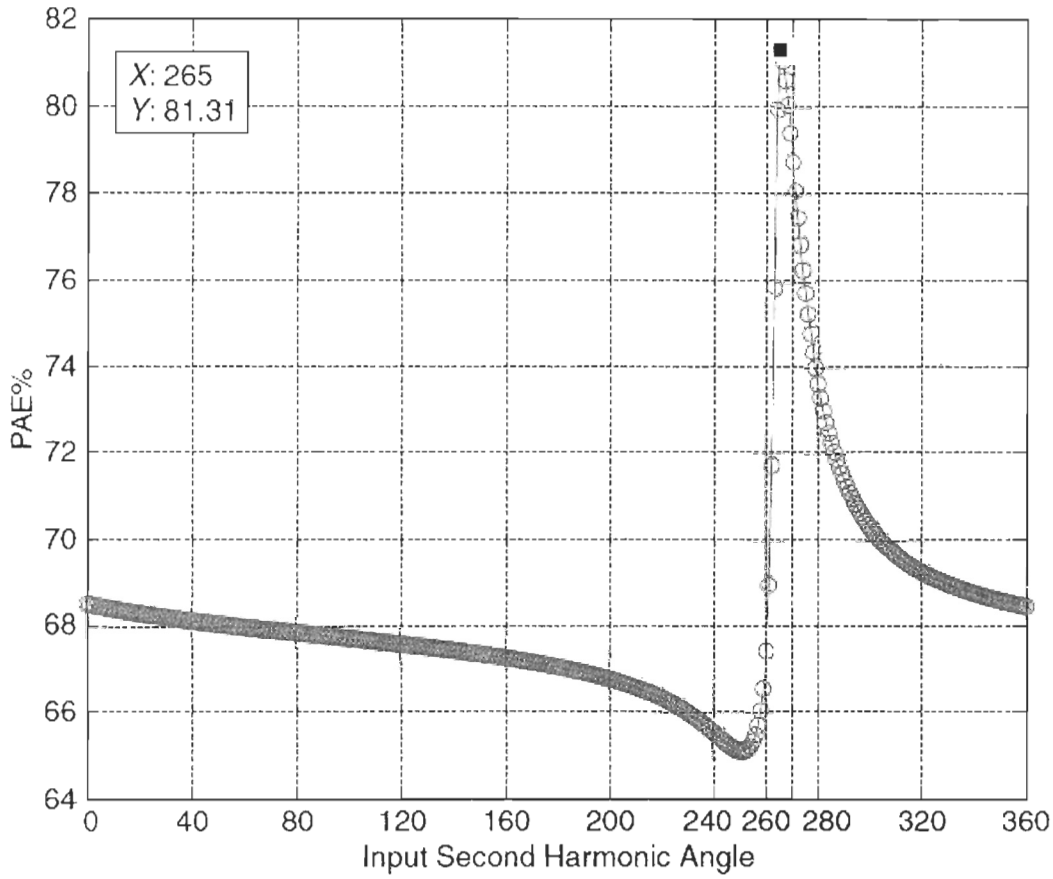


Figure 5 : PAE par rapport à la phase de l'impédance de source à la fréquence 2ème harmonique avec la phase optimale de l'impédance de source à la fréquence 3ème harmonique (Wu *et al.*, 2010a)

1.1.5 Le coefficient de réflexion maximale du tuner passif

L'inconvénient du *tuner* passif est que le coefficient de réflexion (Γ) maximal au niveau du plan de référence DUT obtenu par le *tuner* passif est inférieur à celui du *tuner* actif (inférieur à 1 et typiquement dans la plage de 0.800 à 0.920) en raison de la limite de la sonde et des pertes subies (Agilent technologies Inc., 2011a). Le Γ élevé au plan de référence DUT est important lorsque le transistor est caractérisé pour un fonctionnement de

classe F inverse. Un Γ supérieur pourrait augmenter la puissance de sortie et le PAE d'AP (Wu *et al.*, 2010a).

Afin d'augmenter le valeur maximale de Γ au plan de référence DUT, (Focus microwaves Inc., 1999 et Maury microwave Inc., 2000; cité par Hashmi *et al.*, 2011) introduisent la technologie *pre-matching*. Cette technologie permet d'augmenter la valeur maximale de Γ de 0.750 à 0.900-0.920, en employant deux sondes de radio fréquence (RF) indépendantes dans le *tuner* passif. Cependant, pour un *tuner source/load pull* multi-harmonique, il n'a que 3 sondes. Si nous utilisons cette technologie pour augmenter le Γ pour une fréquence, nous ne pouvons pas contrôler les 3 fréquences en même temps. Ainsi, la question est de savoir comment augmenter la valeur maximale de Γ du *tuner* passif multi-harmonique.

Après avoir montré les problèmes, les objectifs de ce travail sont décrits dans la section 1.2. Basée sur les problématiques et les objectifs, l'hypothèse est faite dans la section 1.3. La méthodologie adoptée pour atteindre les objectifs est déclarée dans la section 1.4.

1.2 OBJECTIFS

L'un des objectifs du projet de recherche est la mise en place d'une conception de premier passage d'AP de classe F inverse avec transistor pour un signal de 1-ton et un signal LTE. Pour ce faire, nous devons

1. Caractériser le transistor avec un signal 1-ton.

2. Caractériser le transistor avec un signal LTE.

3. En se basant sur les résultats de la caractérisation, concevoir et fabriquer les APs de classe F inverse pour un signal 1-ton et un signal LTE.

4. Mesurer les APs de classe F inverse fabriqués et analyser les résultats de la mesure.

Un autre objectif consiste à augmenter le Γ maximal du *tuner source & load pull* passif au niveau du plan de référence DUT.

1.3 HYPOTHÈSE

Basé sur les recherches des autres auteurs mentionnés ci-dessus, nous supposons que le système *source & load pull tuner* peut caractériser le transistor avec plus de précision que le modèle de grand signal. Ainsi, afin de réaliser une conception de premier passage d'AP de classe F inverse pour des signaux 1-ton/LTE, on peut caractériser le transistor par le système *source & load pull tuner* multi-harmonique avec un signal LTE comme le montre la Figure 6.

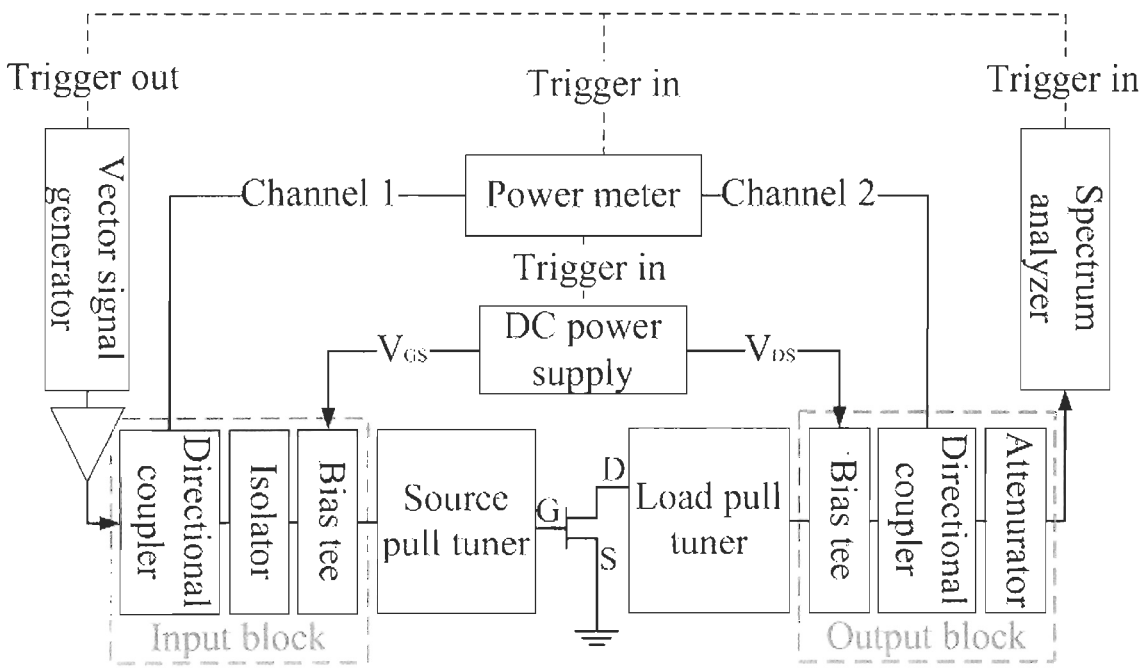


Figure 6 : Configuration pour le système *source & load pull tuner*

Nous supposons également que la performance de l'AP de classe F inverse, comme le PAE et la puissance de sortie, pourrai être affectées par les 2ème et 3ème harmoniques de la source. Ainsi, dans la caractérisation du transistor, les 2ème et 3ème harmoniques sur l'entrée et la sortie du transistor sont pris en compte.

De plus, nous avons constaté que les accessoires, tels que le té de polarisation, l'isolateur et le coupleur directionnel dans la configuration du système *source & load pull tuner* pourrait affecter le coefficient de réflexion Γ maximal du système *source & load pull tuner* multi-harmonique passif. La Figure 7 montre la configuration de *source pull tuner* avec accessoire dans le système *source & load pull tuner*. Les accessoires sont ajoutés sur le côté gauche du *tuner source pull.*

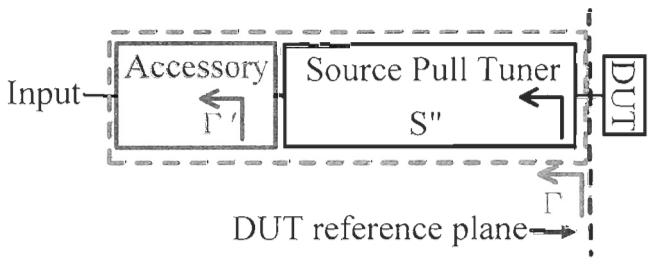


Figure 7 : Configuration pour le *source pull tuner* avec l'accessoire

Le Γ au plan de référence DUT peut être exprimée comme

$$\Gamma = S''_{22} + \frac{S''_{21}S''_{12}\Gamma'}{1 - S''_{11}\Gamma'} \tag{4}$$

où Γ' est le coefficient de réflexion d'accessoires. S'' est le paramètre S du *tuner source pull.* Le paramètre S du DUT est définie comme ci-dessous:

$$S = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \tag{5}$$

où S_{11} est coefficient de réflexion à l'entrée du DUT. S_{12} est coefficient de transmission inverse. S_{21} est coefficient de transmission direct. S_{22} est coefficient de réflexion à la sortie.

De (4), nous pouvons voir que le Γ au plan de référence DUT est affectée par le Γ' des accessoires si le paramètre S du *source pull tuner* est fixé à une valeur. Ainsi, nous supposons que le Γ maximal au plan de référence DUT pourrait être augmenté par le coefficient de réflexion d'accessoires.

1.4 MÉTHODOLOGIE

Pour parvenir à une méthode de conception de premier passage pour la conception AP de classe F inverse utilisant des signaux 1-ton/LTE selon le système *source & load pull tuner*, et de comparer cette méthode avec la méthode de conception par simulation avec le modèle du transistor à grand signal. La méthodologie utilisée dans ce travail est décrite comme suit:

1. Choisir le transistor utilisé dans l'AP de classe F inverse. Dans ce travail, le transistor CGH40010 de Cree Inc. a été utilisé. Le transistor CGH40010 est un transistor à effet de champ.

2. Chercher le modèle du transistor de grand signal. Dans ce travail, le modèle du transistor de grand signal est "CGH40010F_r6_CGH40_r6" de Cree Inc.

3. Choisir la fréquence des signaux 1-ton/LTE pour l'AP de classe F inverse. Dans ce travail, une fréquence de 3.5 GHz est choisie pour le signal de 1-ton. Une fréquence de 3.5 GHz et une largeur de bande de 10 MHz sont choisis pour le signal de LTE.

4. Caractériser le modèle du transistor de grand signal par *source & load pull* simulation dans ADS 2011.10 avec signal 1-ton. Les $2^{ème}$ et $3^{ème}$ harmoniques sur l'entrée et la sortie du transistor sont pris en compte.

5. Caractériser le transistor par le système *source & load pull tuner* multi-harmonique de *Focus microwaves Inc.* avec un signal 1-ton. Les $2^{ème}$ et $3^{ème}$ harmoniques sur l'entrée et la sortie du transistor sont pris en compte.

6. Comparer et analyser les résultats obtenus par simulation de *source & load pull* et le système *source & load pull tuner* de *Focus microwaves Inc.* avec le signal 1-ton.

7. Caractériser le transistor avec le système *source & load pull tuner* multi-harmonique de *Focus microwaves Inc.* pour un signal LTE. Les $2^{ème}$ et $3^{ème}$ harmoniques sur l'entrée et la sortie du transistor sont pris en compte.

8. Concevoir et fabriquer les APs de classe F inverse pour le signal 1-ton et le signal LTE basés sur les résultats des caractérisations. Comparer et analyser les résultats de mesure des APs fabriqués avec les résultats des caractérisations.

1.5 ORGANISATION DU MÉMOIRE

Le mémoire est organisé comme suit: dans le chapitre 2, le transistor CGH40010 de Cree Inc. est caractérisé et analysé pour un signal 1-ton et un signal LTE par la simulation *source & load pull* dans ADS 2011.10 et par le système *source & load pull tuner* de *Focus microwaves Inc.* Les résultats de caractérisation obtenus par la simulation d'ADS et par le système *source & load pull tuner* sont comparés et analysés. Dans le chapitre 3, une méthode pour augmenter le coefficient de réfection (Γ) du *tuner source/load pull* en choisissant des accessoires dans le système *source/load pull tuner* passif est introduite. Dans le chapitre 4, une méthode de conception d'un circuit de polarisation à large bande constituée d'une ligne de transmission avec une longueur de $\lambda/4$ à haute impédance et un *stub* radial pour l'AP de classe F inverse pour un signal de LTE est proposée. Dans le chapitre 5, les APs classe F inverse sont conçus sur la base des résultats de la

caractérisation du chapitre 2. Les résultats mesurés des APs fabriqués sont utilisés pour évaluer les résultats de la caractérisation obtenus. Ce mémoire se termine par la conclusion.

1.6 CONTRIBUTION

Selon la méthode décrite dans la section précédente, pour mettre en place une méthodologie de conception de premier passage d'AP de classe F inverse, nous proposons de caractériser et d'analyser le transistor par l'utilisation du système *source & load pull tuner* multi-harmonique. À notre connaissance, c'est la première fois que le $2^{ème}$ et le $3^{ème}$ harmoniques de la source soient pris en compte dans la caractérisation et l'analyse par le système *source & load pull tuner* multi-harmonique avec un signal 1-ton. Et c'est la première fois également que le système *source & load pull tuner* multi-harmonique est utilisé pour caractériser un transistor avec un signal LTE. En outre, c'est la première fois que les accessoires du système *source & load pull tuner* sont analysés et utilisés pour augmenter le Γ maximal de tuner passif.

Dans toute ma formation de maîtrise, nous avons publié plusieurs articles sur les méthodes de conception d'AP de classe F et d'AP de classe F inverse, la méthode d'utiliser le *tuner source & load pull*. Toutes mes publications dans les conférences scientifiques sont énumérées ci-dessous:

[1] GAO, Shengjie et Chan-Wang PARK. 2012. « Large signal characterization of GaN HEMT transistor by multi-harmonic source & load pull tuner system ». Dans *IEEE ARFTG microwave measurement conference*. (San Diego, CA, 27-30 novembre 2012).

[2] GAO, Shengjie, Zhebin WANG et Chan-Wang PARK. 2012. « Contour method to shift the tunable region of source/load pull tuners in power amplifier characterization ». Dans *IEEE Asia-Pacific microwave conference*. (Kaohsiung, Taiwan, 4-7 décembre 2012).

[3] GAO, Shengjie, Zhebin WANG et Chan-Wang PARK. 2011. « Concurrent dual-band power amplifier with second harmonic controlled by gate and drain bias circuit ». Dans

IEEE International conference on microwave technology & computational electromagnetics. (Beijing, Chine, 22-25 mai 2011), p. 309-312.

[4] GAO, Shengjie et Chan-Wang PARK. 2010. « A Novel method for designing an inverse class F power amplifier by controlling up to fifth harmonic ». Dans *IEEE Asia-Pacific conference on applied electromagnetics*. (Port Dickson, Malaysia, 9-11 novembre 2010), p. 1-4.

[5] GAO, Shengjie, Zhebin WANG et Chan-Wang PARK. 2010. « A novel RF tunable impedance matching network for correcting the tested result deviation from simulated result ». Dans *IEEE Asia-Pacific conference on applied electromagnetics*. (Port Dickson, Malaysia, 9-11 novembre 2010), p. 1-4.

CHAPITRE 2
CHARACTERIZATION OF TRANSISTOR BY THE SOURCE & LOAD PULL SIMULATION IN ADS AND BY THE MULTI-HARMONIC SOURCE & LOAD PULL TUNER SYSTEM

2.1 RÉSUMÉ

Dans ce chapitre, pour concevoir l'amplificateur de puissance classe F inverse, le transistor CGH40010 de Cree Inc. est caractérisé et analysé à 3.5 GHz. La caractérisation et l'analyse sont actionnées par la simulation *source & load pull* dans ADS 2011.10 avec le modèle de transistor CGH40010 à grand signal et par le système *source & load pull tuner* de *Focus microwaves Inc.* $2^{ème}$ et $3^{ème}$ harmoniques d'entrée et de sortie du transistor sont pris en compte lors de la caractérisation. Tout d'abord, nous allons caractériser et analyser le modèle de transistor CGH40010 à grand signal par la simulation *source & load pull* dans ADS pour un signal 1-ton à 3.5 GHz. Ensuite, le transistor CGH40010 est caractérisé par le système *source & load pull tuner* de *Focus microwaves Inc.* pour un signal 1-ton à 3.5 GHz et un signal LTE à 3.5 GHz avec 10 MHz de bande passante. Les résultats de caractérisation obtenus par la simulation d'ADS et par le système *source & load pull tuner* sont comparés et analysés.

2.2 ABSTRACT

In this chapter, in order to achieve a first-pass design methodology for designing the inverse class F power amplifier, the Cree's GaN HEMT CGH40010 transistor is

characterized and analyzed at 3.5 GHz. The characterization and analysis are operated by the source & load pull simulation in ADS 2011.10 with CGH40010's large signal model and by the multi-harmonic source & load pull tuner system from Focus microwaves Inc. The 2^{nd} and 3^{rd} harmonics on both input and output side of the transistor are considered during the characterization. First, the CGH40010 transistor's large signal model is characterized and analyzed by the source & load pull simulation in ADS with 1-tone signal at 3.5 GHz. Then, the Cree's CGH40010 transistor is characterized and analyzed by Focus microwaves' multi-harmonic source & load pull tuner system with 1-tone signal at 3.5 GHz and LTE signal at 3.5 GHz with 10 MHz bandwidth. The characterization results obtained by the ADS simulation with the large signal model and by the source & load pull tuner system with 1-tone and LTE signal are compared and analyzed.

2.3 INTRODUCTION

With the development of the modern telecommunication technology, such as long term evolution (LTE) and LTE-Advanced, the requirement for the PA with respect to the power added efficiency (PAE) and output power is more stringent. For satisfying the increasing demand of the wireless communication technology, transistor, as a key active device in the PA, should be well characterized. The large signal characterization for the transistor is essential to estimate the output power, the PAE and the linearity in the non-linear domain to achieve a high efficiency PA. From the angle of the PA manufacturing industry, based on (Wu *et al.*, 2010a), high efficiency PAs have not been fabricated on a large scale because of lack of the first-pass design methodology. Practical PA designs are often empirical in nature. To achieve the desired results of a PA, experience and extensive post-production tuning are used. However, for mass production in the PA's industry, this method cannot be used, since the post-production tuning is expensive. The first-pass design methodology could help the industry to fabricate the high efficiency PAs in mass production without post-production tuning.

To achieve a first-pass design methodology for designing a LTE inverse class F PA, the transistor should be characterized in non-linear region at fundamental, the 2nd and 3rd harmonic frequencies. In the previous researches of other authors, the PA is usually designed with the large signal transistor model.

In Moon's work (Moon *et al.*, 2011), a PA for a LTE signal with Cree's gallium nitride high electron mobility transistor (GaN HEMT) CGH40010 is presented. The PA is designed based on the 1-tone characterization by simulation with the large signal transistor model. The fabricated PA without digital predistortion (DPD) linearization could offer 29.05% PAE when the output power is 34.99 dBm, the gain is 13.29 dB and the adjacent channel power ratio ACPR1/ACPR2 at 7.5/12.5 MHz offset is -25.14/-32.24 dBc when the PA is measured with a 10 MHz bandwidth LTE signal at 1.84 GHz.

In (Kim *et al.*, 2010b), a saturated multi-band PA is presented. The multi-band PA is designed based on the 1-tone characterization result obtained by the simulation with the large signal transistor model of the Cree's CGH40015 transistor at 1.85 GHz, 1.96 GHz and 2.14 GHz. With a 10 MHz bandwidth LTE signal at 2.14 GHz, the drain efficiency is 34.40% when the output power is 36.10 dBm and the ACPR is -29.40 dBc without DPD linearization.

In (Markos *et al.*, 2010), a 50W unsymmetrical Doherty PA is realized to be operated at 2.5 GHz. The PA is designed based on the 1-tone characterization result obtained by simulation with large signal transistor model. With a 10 MHz bandwidth LTE signal at 2.5 GHz, 48.00% PAE was measured with 47.00 dBm output power when ACPR is -35.00 dBc before DPD linearization.

As previously mentioned, large signal transistor models are generally used to design PAs. However, the problem is that sometimes transistor model is not accurate enough when the transistor is excited with large signal based on our experience and the other authors (Jung *et al.*, 2009; De Groote *et al.*, 2007). Thus, the question is how we can characterize the transistor accurately with LTE signal.

The main objective in this work is to find a first-pass design methodology to design an inverse class F PAs in the LTE base station in Europe. To do that, the transistor should be characterized precisely. However, we found that the large signal model is not accurate enough with large signal.

To solve this problem, the source & load pull tuner is recommended to be used in the transistor characterization (Colantonio *et al.*, 2009). By using the multi-harmonic source & load pull tuner, RF parameters of the transistor, such as the output power, the PAE, etc. could be measured directly and accurately when the load and source impedances at fundamental, the 2nd and 3rd harmonic frequencies are controlled (Liu *et al.*, 2003). Previous researches (Ghannouchi *et al.*, 2009; De Groote *et al.*, 2007; Fennelly *et al.*, 1997; Deshours *et al.*, 1997; Ghannouchi *et al.*, 1994) show that the transistor can be characterized precisely under 1-tone, 2-tone and CDMA excitation by using the source & load pull tuner. However, in their works, they only considered the 2^{nd} and 3^{rd} harmonic on the output side of the transistor (load 2^{nd} and 3^{rd} harmonics) as shown in Table 2 in section 1.1.3. Wu indicates that the PAE is also sensitive to the 2^{nd} harmonic on the input side of the transistor, so the 2^{nd} and 3^{rd} harmonic on the input side of the transistor (source 2^{nd} and 3^{rd} harmonic) should be considered (Wu *et al.*, 2010a).

The original idea is to characterize the transistor by the tuner system when the transistor is excited with the large signal. The source and load 2^{nd} and 3^{rd} harmonics are considered during the characterization. In order to control the source and load impedances at the 2^{nd} and 3^{rd} harmonic frequencies, iMPT-1818-TC source & load pull tuners developed by Focus microwaves Inc. are used. This tuner can tune the source and load impedances at fundamental, the 2^{nd} and 3^{rd} harmonic frequencies independently (Focus microwaves Inc., 2007). Thus, by this multi-harmonic source & load pull tuner, the transistor could be characterized and analyzed precisely to achieve a first-pass design methodology for the inverse class F PA.

To achieve this methodology, in section 2.3 and 2.4, our original approach for characterizing and analyzing the transistor by the multi-harmonic source & load pull tuner

system is shown with the Cree's CGH40010 transistor. The large signal model of the CGH40010 transistor provide by Cree Inc. is also used in this chapter to characterize and analyze this transistor by the 1-tone source & load pull simulation in ADS. In this way, the 1-tone characterization results obtained by the simulation and by the multi-harmonic tuner system can be compared.

The objective in this chapter is to characterize the CGH40010 transistor with large signal for the inverse class F PAs used in the LTE base station in Europe. The allocated center frequency of LTE signal in the base station of Europe is 3.5 GHz (Motorola Inc., 2012). Therefore, the fundamental frequency for the inverse class F PA is fixed to 3.5 GHz. The procedures for analyzing the CGH40010 transistor are described as follows:

1. In section 2.4, first, the CGH40010 transistor is characterized and analyzed first by the source & load pull simulation in ADS 2011.10 with transistor's large signal model for the 1-tone signal at 3.5 GHz. Then, the CGH40010 transistor is characterized and analyzed by the multi-harmonic source & load pull tuner system from Focus microwaves Inc. for the 1-tone signal at 3.5 GHz. The 2^{nd} and 3^{rd} harmonics on both input and output side of the transistor are considered.

2. In section 2.5, the CGH40010 transistor is characterized and analyzed by the multi-harmonic source & load pull tuner system from Focus microwaves Inc. for the 10 MHz bandwidth LTE signal at 3.5 GHz. The 2^{nd} and 3^{rd} harmonics on both input and output side of the transistor are considered.

3. The results obtained in the characterizations are compared and analyzed.

2.4 PROPOSED METHOD FOR 1-TONE CHARACTERIZATION OF CGH40010 TRANSISTOR

In this part, the methods for the 1-tone characterization of CGH40010 transistor at 3.5 GHz are proposed. The 2^{nd} and 3^{rd} harmonics on both input and output side of the transistor

are considered in the 1-tone characterizations. The source & load pull simulation in ADS 2011.10 and the multi-harmonic source & load pull tuner system are used to characterize this transistor with 1-tone signal at 3.5 GHz. The structure of this section is organized as follows:

1. In section 2.4.1, the method of characterizing and analyzing CGH40010 transistor by the source & load pull simulation in ADS with the large signal transistor model for the 1-tone signal at 3.5 GHz is proposed.

2. In section 2.4.2, the method of characterizing and analyzing CGH40010 transistor by the multi-harmonic source & load pull tuner system for the 1-tone signal at 3.5 GHz is proposed.

3. In section 2.4.3, the 1-tone characterization results obtained by the simulation and by the tuner system are compared and analyzed.

2.4.1 Proposed method of 1-tone characterization for CGH40010 transistor by the simulation with large signal model

In this section, the methods for characterizing the 10W device CGH40010 transistor by the source & load pull simulation in ADS 2011.10 with transistor's large signal model for a 1-tone signal at 3.5 GHz are proposed. The large signal model of CGH40010 transistor "CGH40010F_r6_CGH40_r6" provided by Cree Inc. is used in the characterization by the simulation in ADS. Two characterization methods by the source & load pull simulation in ADS, labeled as method no. 1 and method no. 2, are proposed. Section 2.3.1.1 shows the simulation method no. 1 which employs the design guides named "One Tone, Constant Available Source Power Load Pull" and "One Tone, Constant Available Source Power Source Pull" in ADS 2011.10. Section 2.3.1.2 shows the simulation method no. 2 which employs the design guides named "Load-Pull-PAE, Output Power Contours" and "Source-Pull-PAE, Output Power Contours".

The objective of the 1-tone characterizations for the CGH40010 transistor by two methods is obtaining the maximum PAE when the output power is more than 40 dBm at 3.5 GHz with 25 dBm input power.

The schematic of the I-V curve simulation and simulated I-V curve of CGH40010 transistor is shown in Figure 8. For an inverse class F operation, the transistor can be biased in class AB mode (Wu *et al.*, 2009), so we choose to bias the transistor at V_{DS}=28 V and V_{GS}=-2.73 V with 200 mA quiescent drain current as a class AB operation.

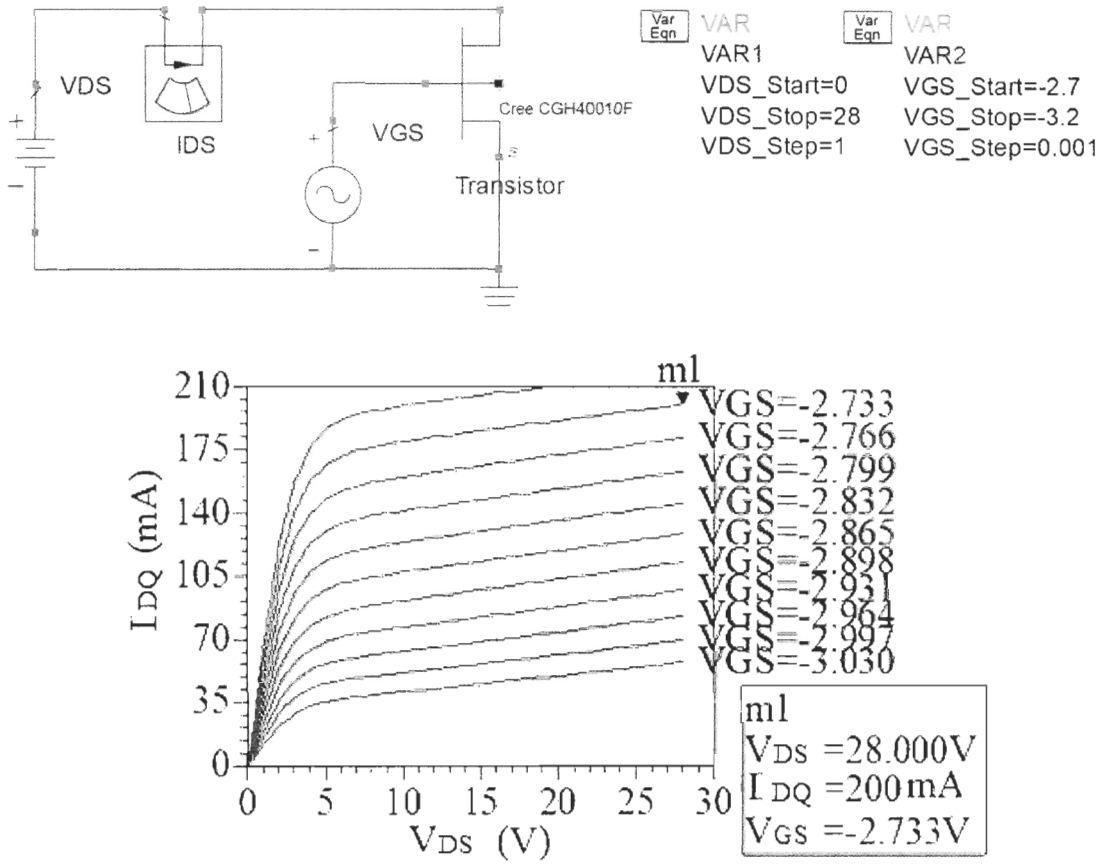


Figure 8 : Schematic of the I-V curve simulation and the simulated I-V curve in ADS with CGH40010 transistor's large signal model

After fixing the bias condition, the simulated stability circles of CGH40010 transistor at 3.5 GHz, 7 GHz and 10.5 GHz are as shown in Figure 9.

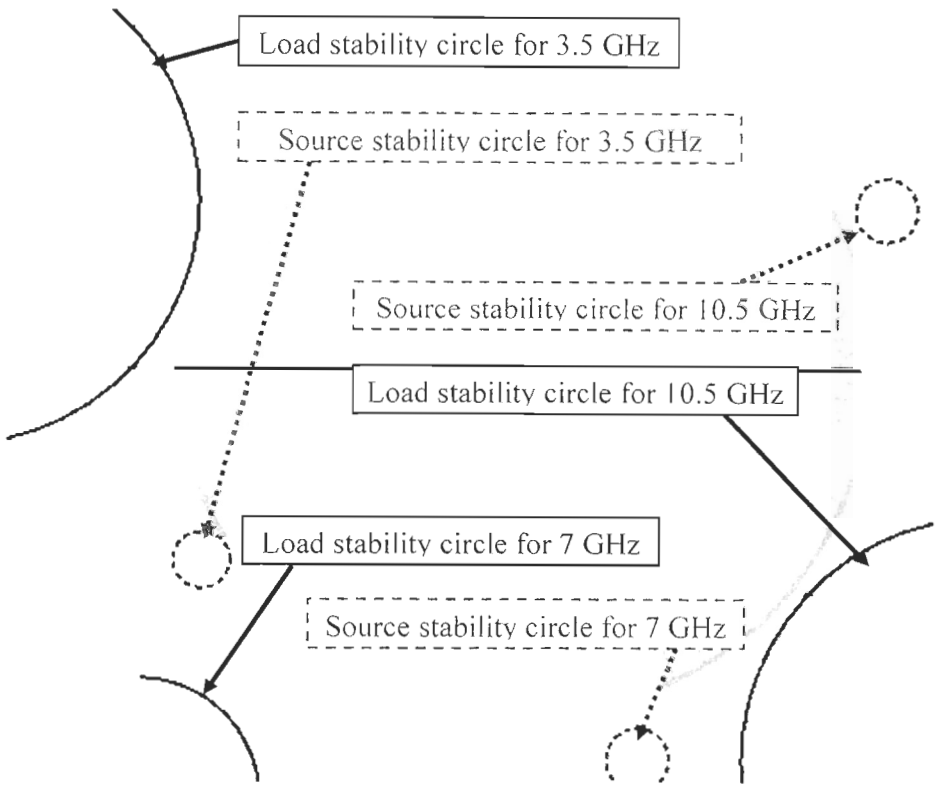


Figure 9 : Simulated stability circles in ADS with CGH40010 transistor's large signal model for 3.5 GHz, 7 GHz and 10.5 GHz.

From the simulation results in Figure 9, we can see that the source and load stability circles do not overlap with the Smith chart, so the transistor is unconditionally stable (Gonzalez, 1996 : 219).

2.4.1.1 Proposed procedure for the 1-tone characterization by simulation method no. 1

The proposed procedure of the 1-tone characterization by simulation method no.1 is presented in this section. The first method to characterize the CGH40010 transistor at 3.5 GHz, labeled as method no. 1, uses the design guide named "One Tone, Constant Available Source Power Load Pull" and "One Tone, Constant Available Source Power Source Pull"

in ADS 2011.10. During the characterization by the simulation method no. 1, the bias condition is fixed to V_{DS}=28 V and V_{GS}=-2.73 V. Input power is fixed to 25 dBm.

As a first step, source fundamental impedance is fixed to 3.18-j13.30 Ω which is recommended in the data sheet of the Cree's CGH40010 transistor at 3.5 GHz (Cree Inc., 2012). The impedance 3.18-j13.30 Ω also can be expressed as $0.888\angle$-150.1° by the calculation as follows (Gonzalez, 1996 : 93),

$$\Gamma = \frac{Z - Z_0}{Z + Z_0} \tag{6}$$

where Z is the source impedance at fundamental frequency. Z_0 is the characteristic impedance. In this memoire, Z_0 = 50 Ω and all the impedances are not normalized. In this memoire, Γ is also used to present the impedance. The source and load impedances at the 2nd and 3rd harmonic frequencies are 50 Ω. The load pull simulation result in Figure 10 shows that the maximum PAE obtained in the load pull simulation is 65.23% with 40.33 dBm output power when the load impedance is $0.566\angle$161.7°. The maximum output power is 41.17 dBm with 59.11% PAE when the impedance is $0.547\angle$-177.2°. In order to have more than 40 dBm output power and pursue higher PAE, the maximum PAE impedance of $0.566\angle$161.7° is chosen.

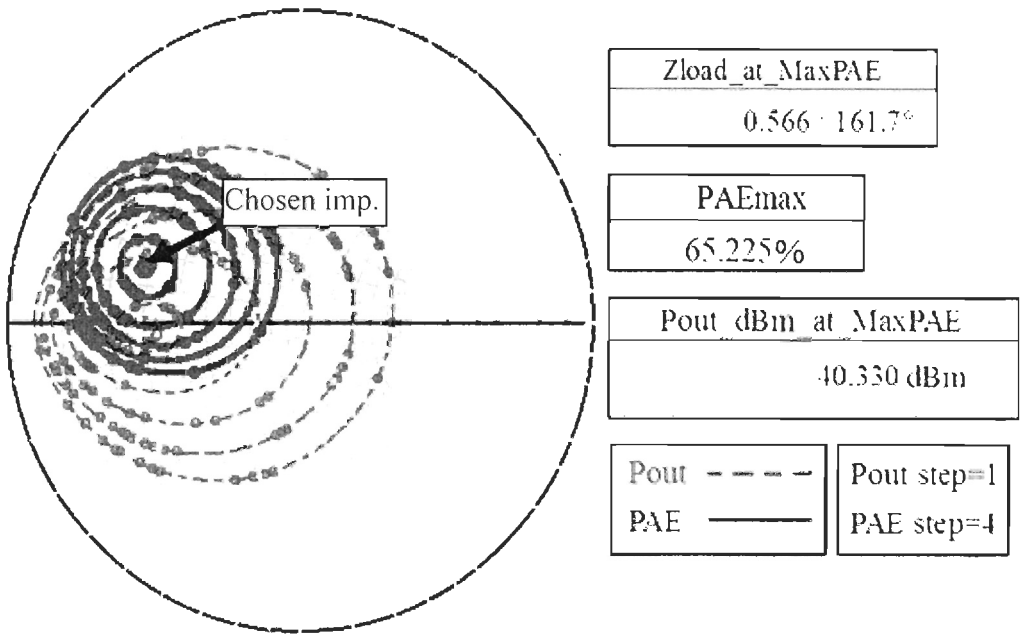


Figure 10 : Simulated PAE and output power contour by the load pull simulation in ADS at 3.5 GH

Then, as a second step, source pull simulation is operated for the source impedance at 3.5 GHz when the load impedance at 3.5 GHz is fixed to 0.566∠161.7°. The source and load impedances at the 2nd and 3rd harmonic frequencies are 50 Ω. The source pull simulation results in Figure 11shows that the maximum PAE is 66.36% with 40.54 dBm output power when the source impedance at 3.5 GHz is 0.941∠-151.8°. The maximum output power is 40.55 dBm with 66.33% PAE when the source impedance at fundamental frequency is 0.941∠-152.1°. In order to have more than 40 dBm output power and pursue higher PAE, the maximum PAE impedance of 0.941∠-151.8° is chosen.

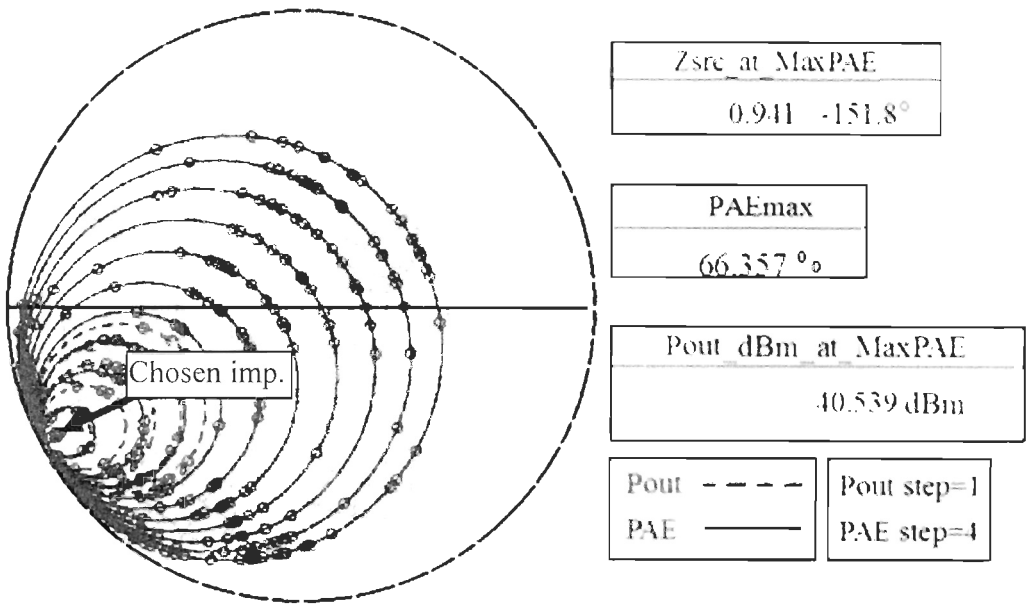
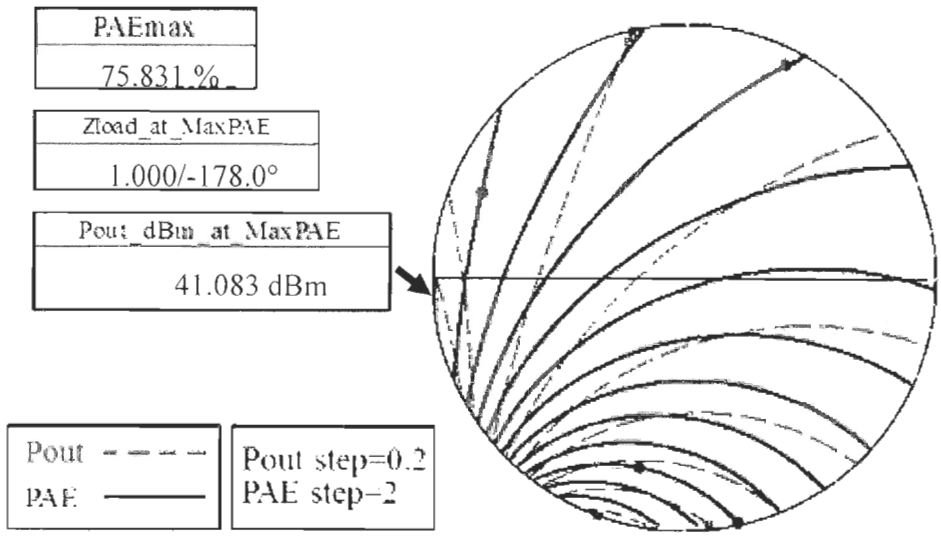
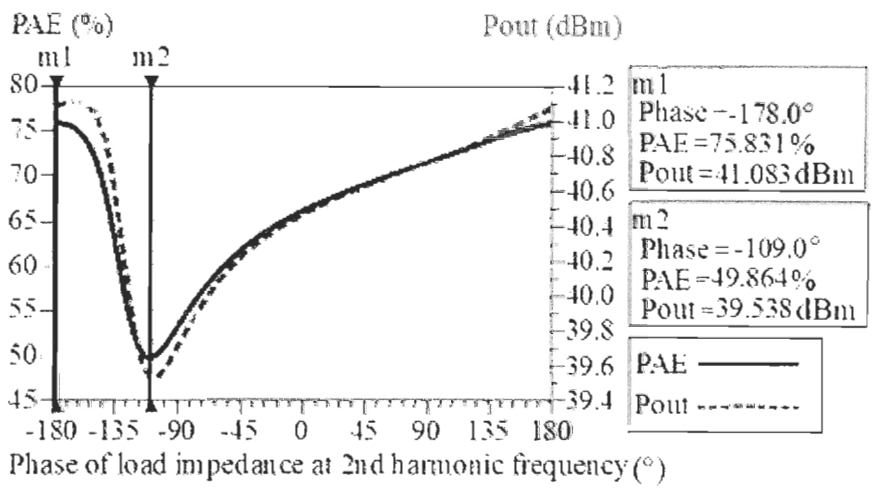


Figure 11 : Simulated PAE and output power contour by the source pull simulation in ADS at 3.5 GHz

Next step is tuning the load impedance at the 2nd harmonic frequency (7 GHz) when the source and load impedances at 3.5GHz are fixed to 0.566∠161.7° and 0.941∠-151.8°, respectively. The source impedances at the 2nd and 3rd harmonic frequencies and load impedance at the 3rd harmonic frequency are fixed to 50 Ω. Figure 12 (a) shows the simulated PAE and output power contour when the load impedance at 7 GHz is tuned. The maximum PAE of 75.83% with 41.08 dBm output power is found when the load impedance at 7 GHz is 1.000∠-178.0°. In this step, 9.47% PAE can be increased by controlling the load impedance at the 2nd harmonic frequency. Figure 12 (b) shows the simulated PAE and output power when the phase of the load impedance at 7 GHz is changed from -180° to 180° with the Γ of the load impedance at 7 GHz fixed to 1. From Figure 12 (b), we can see that if the phase of the load impedance at 7 GHz is -109.0° (m2 in Figure 12 (b)), the PAE is reduced to the minimum value of 49.86% with 39.54 dBm output power. Thus, the load impedance at 7 GHz is important for an inverse class F PA to achieve a high PAE and more than 40 dBm output power.



(a)



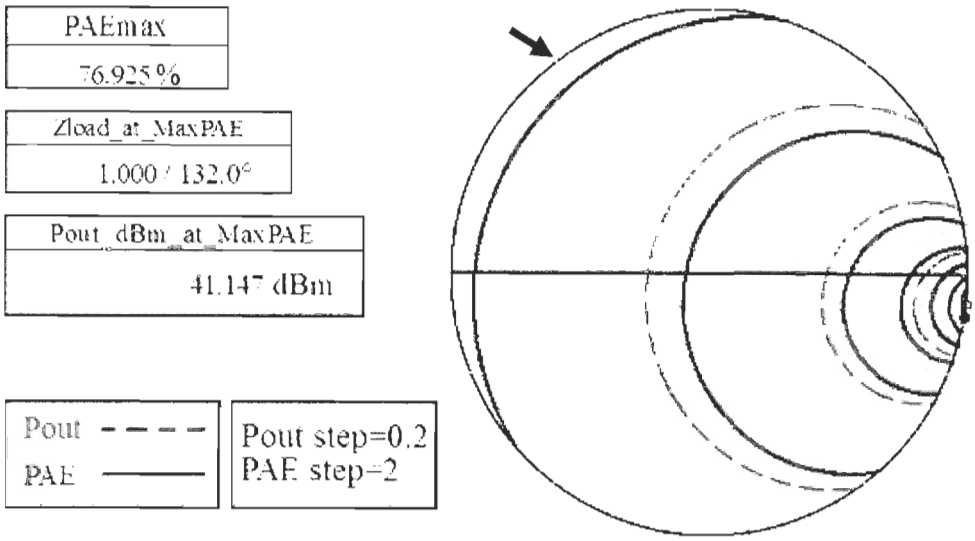
(b)

Figure 12 : Simulated PAE and output power contour on Smith Chart (a) and the simulated PAE and output power versus the phase of the load impedance at the 2nd harmonic frequency (b) by method no. 1

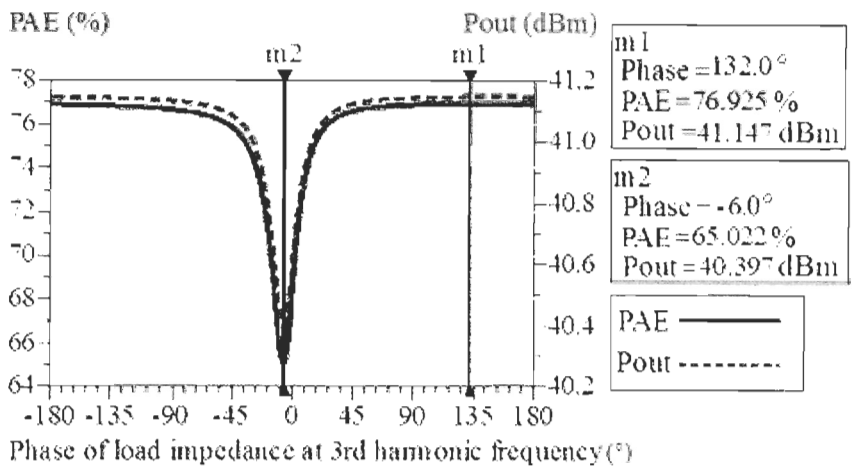
As a fourth step, the load impedance at the 3rd harmonic frequency (10.5 GHz) is tuned while the source and load impedances at fundamental frequency are fixed to 0.566∠ 161.7° and 0.941∠-151.8°, respectively. The load impedance at the 2nd harmonic is fixed to 1.000∠-178.0°. The simulation result in Figure 13 (a) indicates that when the impedance

of 3rd harmonic is 1.000∠132.0°, the PAE reaches the maximum value of 76.93% with 41.15 dBm output power. In this step, the PAE is increased from 75.83% to 76.93% by tuning the load impedance at the 3rd harmonic frequency from 50 Ω to 1.000∠132.0°. Figure 13 (b) shows the simulated PAE and output power when the phase of the load impedance at 10.5 GHz is changed from -180° to 180° with the Γ of the load impedance at 10.5 GHz fixed to 1. If the phase of the load impedance at the 3rd harmonic frequency is -6.0° (m2 in Figure 13 (b)), the PAE is reduced to the minimum value 65.02% when output power is 40.40 dBm. Thus, the load impedance at the 3rd harmonic is also important for an inverse class F PA to achieve a high PAE and more than 40 dBm output power.

By only controlling the load impedances at the 2nd and 3rd harmonics, the PAE is increased from 66.36% to 76.93% while the output power is maintained more than 40 dBm. From the simulation results in Figure 12 (a) and Figure 13 (a), we can see that the Γ of the load impedances at the 2nd and 3rd harmonic frequencies which offers the maximum PAE always equals to 1. In other words, the 2nd and 3rd harmonic frequencies on the output side of the transistor should be reflected or suppressed to achieve a high PAE. By analyzing the simulation results in Figure 12 (b) and Figure 13 (b), we can see that if there is 69.0° difference in phase of the load impedance at the 2nd harmonic frequency, the PAE could be reduced by 25.97%. If there is 138.0° difference in phase of the load impedance at the 3rd harmonic frequency, the PAE could be reduced by 11.73%. Thus, besides of the Γ of the load impedance at the 2nd and 3rd harmonic frequencies, the phases of load impedance at the 2nd and 3rd harmonic frequencies are also important to provide a high PAE for an inverse class F PA.



(a)



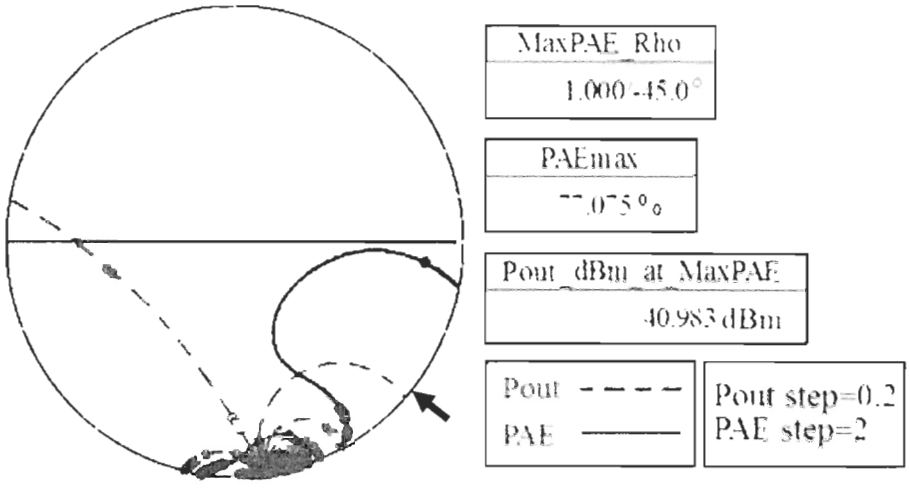
(b)

Figure 13 : Simulated PAE and output power contour on Smith chart (a) and the simulated PAE and output power versus the phase of the load impedance at the 3rd harmonic frequency (b) by method no. 1

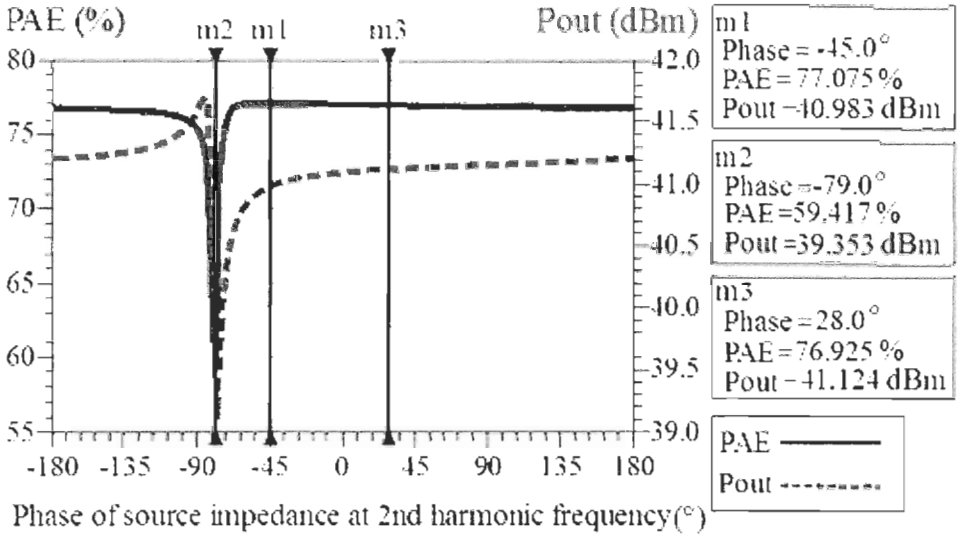
The next step is tuning the source impedance at the 2nd harmonic frequency. The source and load impedances at fundamental frequency are fixed to $0.566 \angle 161.7°$ and $0.941 \angle -151.8°$, respectively. The load impedances at the 2nd and 3rd harmonic frequencies are fixed to $1.000 \angle -178.0°$ and $1.000 \angle 132.0°$. The source impedance at the 3rd harmonic frequency is fixed to 50 Ω.

The simulation results in Figure 14 (a) show that when the source impedance at the 2nd harmonic frequency is 1.000∠-45.0°, the maximum PAE of 77.08% can be obtained with 40.98 dBm output power. The maximum PAE can only be increased by 0.15% in this step. Figure 14 (b) shows the simulated PAE and output power when the phase of the source impedance at 7 GHz is changed from -180° to 180° with the Γ of the source impedance at 7 GHz fixed to 1. From Figure 14 (b), we can see that the PAE is sensitive to the phase of the source impedance at the 2nd harmonic frequency. If the phase of the source impedance at the 2nd harmonic frequency is -79.0° (m2 in Figure 14 (b)), the PAE is reduced from the maximum PAE of 77.08% to 59.42%. The similar phenomenon is also described in (Wu *et al.*, 2010a).

By considering the tolerance in the fabrication of the PA circuit which may cause the shift of the phase of the source impedance at the 2nd harmonic frequency, the phase of the source impedance at the 2nd harmonic frequency is chosen away from the region with the PAE fluctuation, such as the region near -79.0°. Thus, 28.0° is chosen for the phase of the source impedance at the 2nd harmonic frequency, instead of the phase which provides the maximum PAE. With this source impedance at the 2nd harmonic frequency, the PAE is maintained at 76.93% with 41.12 dBm output power (m3 in Figure 14 (b)).



(a)

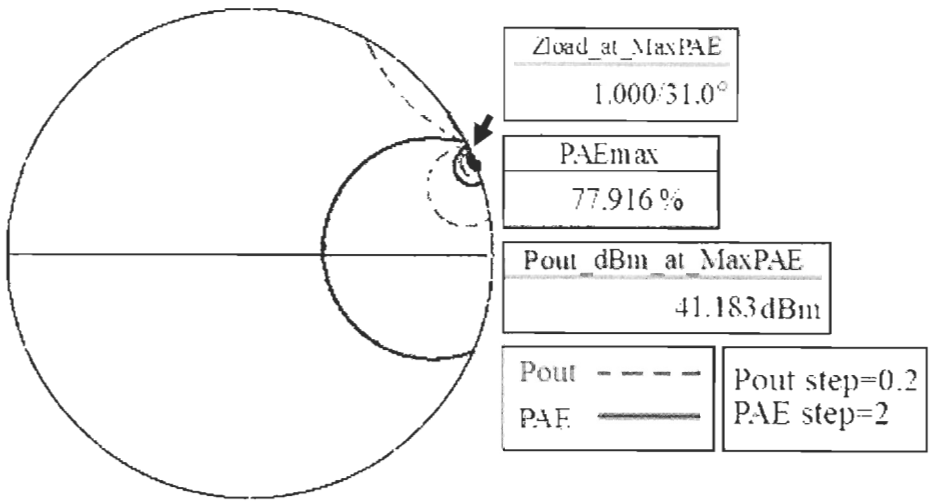


(b)

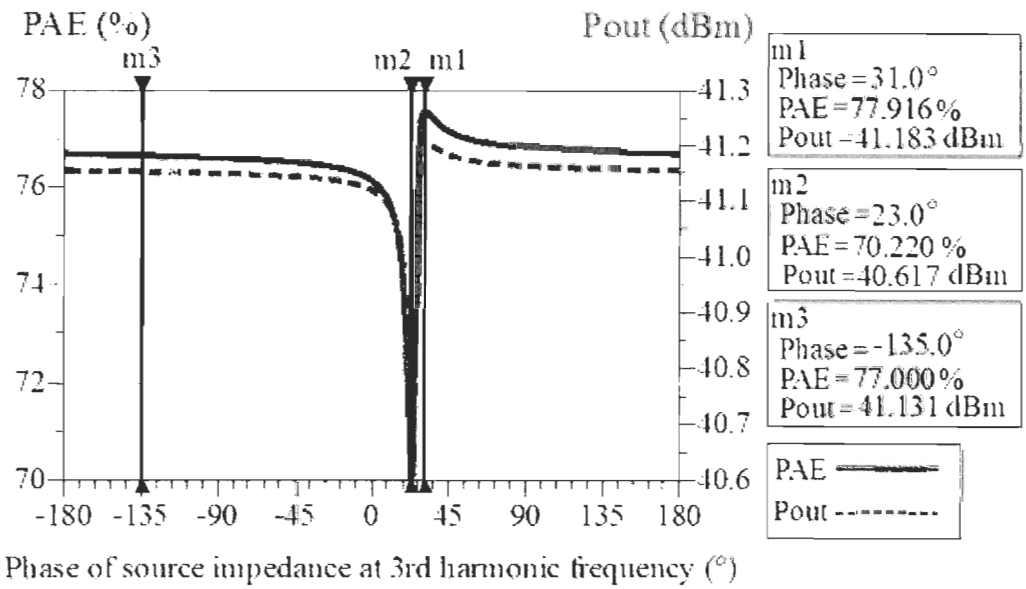
Figure 14 : Simulated PAE and output power contour (a) and the simulated PAE and output power versus the phase of the source impedance at the 2nd harmonic frequency (b) by method no. 1

At last, the source impedance at the 3rd harmonic is tuned. The source and load impedances at fundamental frequency are fixed to $0.566\angle 161.7°$ and $0.941\angle -151.8°$, respectively. The load impedances at the 2nd and 3rd harmonic frequencies are fixed to

$1.000\angle$-178.0° and $1.000\angle$132.0°, respectively. The source impedance at the 3rd harmonic frequency is fixed to $1.000\angle$28.0°. The simulation results are shown in Figure 15. By tuning the source impedance at the 3rd harmonic frequency from 50 Ω to $1.000\angle$31.0°, the maximum PAE is increased from 76.93% to 77.92% with 41.18 dBm output power. The maximum PAE in this step can only be increased by 0.99%. Figure 15 (b) shows the simulated PAE and output power when the phase of the source impedance at 10.5 GHz is changed from -180° to 180° with the Γ of the source impedance at 10.5 GHz fixed to 1. From Figure 15 (b), we can see that the PAE is also sensitive to the phase of the source impedance at the 3rd harmonic frequency when the Γ of source impedance at the 3rd harmonic frequency is 1. If the phase is 23.0°, the PAE could be reduced from the maximum PAE 77.92% to 70.22% (m2 in Figure 15 (b)). 7.70% PAE can be reduced if there is 8.0° difference in phase. Thus, the region with the PAE fluctuation, such as the region near 23.0° should be avoided. -135.0° is chosen for the phase of the source impedance at source 3rd harmonic frequency. When the phase is -135.0°, the PAE is 77.00% with 41.13 dBm output power (m3 in Figure 15 (b)). In this step, the chosen source impedance at the 3rd harmonic frequency increases the PAE by 0.07%.



(a)



(b)

Figure 15 : Simulated PAE and output power contour (a) and the simulated PAE and output power versus the phase of the source impedance at the 3rd harmonic frequency (b) by method no. 1

With this proposed characterization procedure, the chosen source and load impedances at fundamental frequency, the 2nd harmonic and 3rd harmonic frequencies could offer 77.00% PAE and 41.13 dBm output power.

Table 3 summarizes the procedure of 1-tone characterization by the source & load pull simulation with method no. 1. PAE is increased by 9.47% by tuning the load impedance at the 2nd harmonic frequency. By tuning the load impedance at the 3rd harmonic frequency, the PAE is increased by 1.10%. Tuning the source impedances at the 2nd and 3rd harmonic does not improve the PAE significantly compared with the load impedance at the 2nd and 3rd harmonics. Only 0.07% is increased in PAE. However, the PAE is sensitive to the phase of the source impedances at the 2nd and 3rd harmonic frequencies. If the phases of the source impedances at the 2nd and 3rd harmonic frequencies are not well chosen, the PAE could be reduced by a maximum value of 17.66%. Thus, the source impedances at the 2nd and 3rd harmonic frequencies should be well matched when we design the inverse class F PA in case they reduce the PAE. From Table 3, we also can see that the impedances at harmonic frequencies for the maximum PAE are always on the edge of the Smith chart, which means that the harmonic frequencies should be suppressed or reflected to obtain high PAE. Therefore, the input and output impedance matching network of the inverse class F PA should be designed to suppress or reflect the 2nd and 3rd harmonic frequencies. In other words, the Γ of the impedances of the impedance matching network at harmonic frequencies should be designed as near 1 as possible.

Table 3 : 1-tone characterization results obtained by the source & load pull simulation with method no. 1

	Frequency (GHz)	Source impedance	Load impedance	PAE (%)	P_{out} (dBm)
Step 1 Load pull @ 3.5 GHz	3.5	0.888∠-150.1°	0.566∠161.7°	65.23	40.33
	7	0∠0°	0∠0°		
	10.5	0∠0°	0∠0°		
Step 2 Source pull @ 3.5 GHz	3.5	0.941∠-151.8°	0.566∠161.7°	66.36	40.54
	7	0∠0°	0∠0°		
	10.5	0∠0°	0∠0°		
Step 3 Load pull @ 7 GHz	3.5	0.941∠-151.8°	0.566∠161.7°	75.83	41.08
	7	0∠0°	1.000∠-178.0°		
	10.5	0∠0°	0∠0°		
Step 4 Load pull @ 10.5 GHz	3.5	0.941∠-151.8°	0.566∠161.7°	76.93	41.15
	7	0∠0°	1.000∠-178.0°		
	10.5	0∠0°	1.000∠132.0°		
Step 5 Source pull @ 7 GHz	3.5	0.941∠-151.8°	0.566∠161.7°	76.93	41.12
	7	1.000∠28.0°	1.000∠-178.0°		
	10.5	0∠0°	1.000∠132.0°		
Step 6 Source pull @ 10.5 GHz	3.5	0.941∠-151.8°	0.566∠161.7°	77.00	41.13
	7	1.000∠28.0°	1.000∠-178.0°		
	10.5	1.000∠-135.0°	1.000∠132.0°		

2.4.1.2 Proposed procedure for the 1-tone characterization by simulation method no. 2

The second method to characterize the transistor, defined as method no. 2, is using design guide named "Load-Pull-PAE, Output Power Contours" and "Source-Pull-PAE, Output Power Contours" in "1-Tone Nonlinear Simulation" for "Amplifier" in ADS 2011.10. During the characterization by simulation, the bias condition is fixed to V_{DS}=28 V and V_{GS}=-2.73 V. The input power is fixed to 25 dBm. For the characterization procedure with method no. 2, the first two steps for locating the source and load impedance at fundamental frequency (3.5 GHz) are same as the procedure with method no. 1, so the

source impedance and load impedance at 3.5 GHz found by source and load pull simulation are 0.941∠-151.8°and 0.566∠161.7°, respectively.

As a third step, the method for finding the impedance at the 2nd harmonic frequency is different from the method no. 1. First, in the simulation setup, the source impedance at 3.5 GHz is fixed to 0.941∠-151.8°. The load impedance at 10.5 GHz, the source and load impedances at 7 and 10.5 GHz are fixed to 50 Ω. Then, fix the Γ of load impedance at 7 GHz to 1, and change the phase of the load impedance at 7 GHz from -180° to 180° with 1° step. With different values of the phase, the load pull simulation at 3.5 GHz is operated. From each load pull simulation results, we choose the impedance at 3.5 GHz which offers the maximum PAE and record the corresponding PAE and output power. With this method, the simulated maximum PAE and output power as a function of the phase of the load impedance at 7 GHz is shown in Figure 16. The simulation shows that the PAE is increased to a maximum value of 77.71% with 40.41 dBm output power by changing the phase of the load impedance at 7 GHz to 144.0°. The minimum PAE of 58.96% with 40.75 dBm output power is found when the phase is -100.0°. Thus, with method no. 2, we also can say that the phase of the load 2nd harmonic is important to achieve a high PAE.

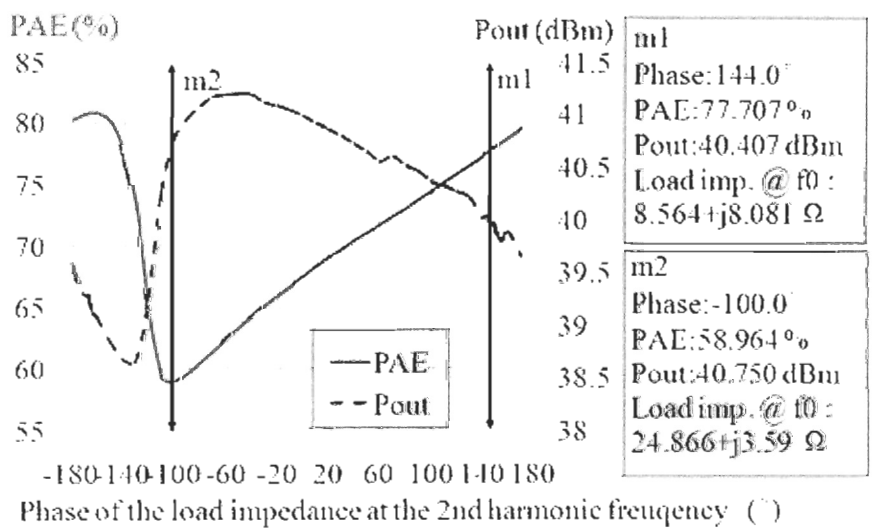


Figure 16 : Simulated PAE and output power versus the phase of the load impedance at the 2nd harmonic frequency by method no. 2

Simulation result in Figure 16 also shows that the load impedance at fundamental frequency which offers 77.71% PAE and 40.41 dBm output power is changed from 0.566 ∠161.7° to 0.714∠161.1° when the phase of the load impedance at the 2nd harmonic frequency is tuned from the center of Smith chart to 1.000∠144.0°. These impedances can be expressed as 14.20+j7.42 Ω and 8.56+j8.08 Ω by (6), respectively. The impedances between 14.20+j7.42 Ω and 8.56+j8.08 Ω with same interval between each other as shown in Figure 17 are chosen to help us understand how the load impedance at 3.5 GHz affects the PAE and output power. In this analysis, the design guide named "One Tone, Load Harmonic Phase Sweep" is used.

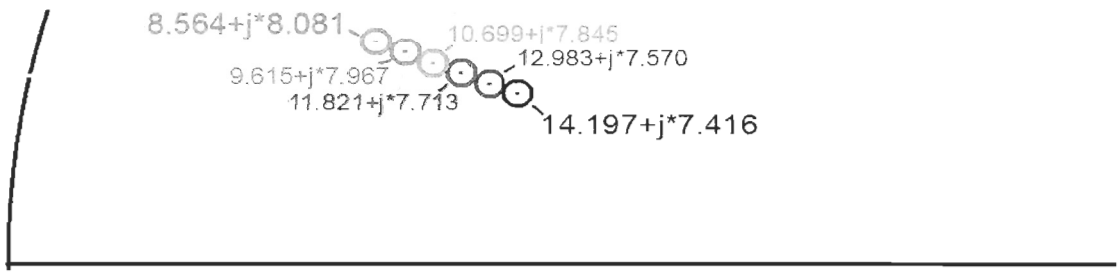
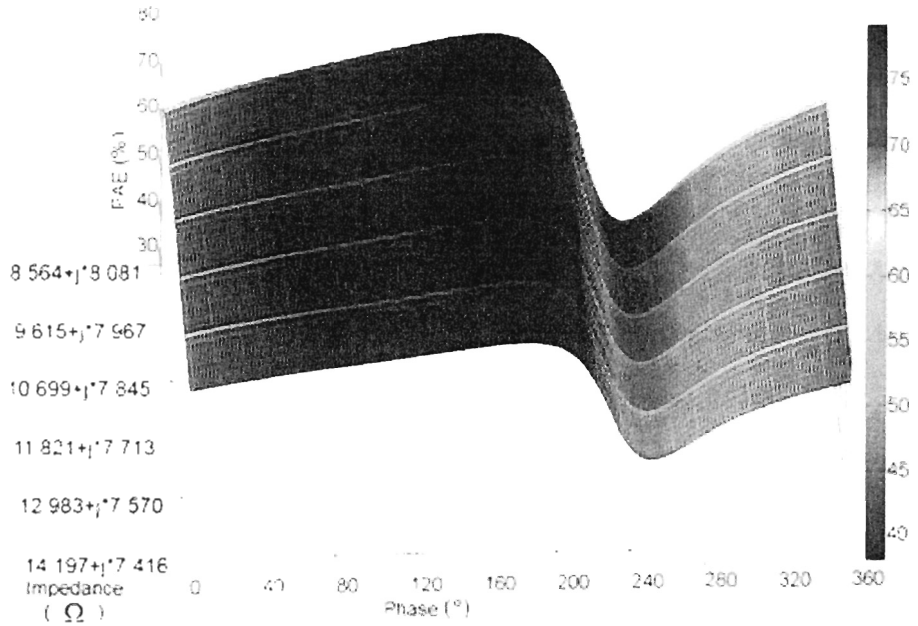
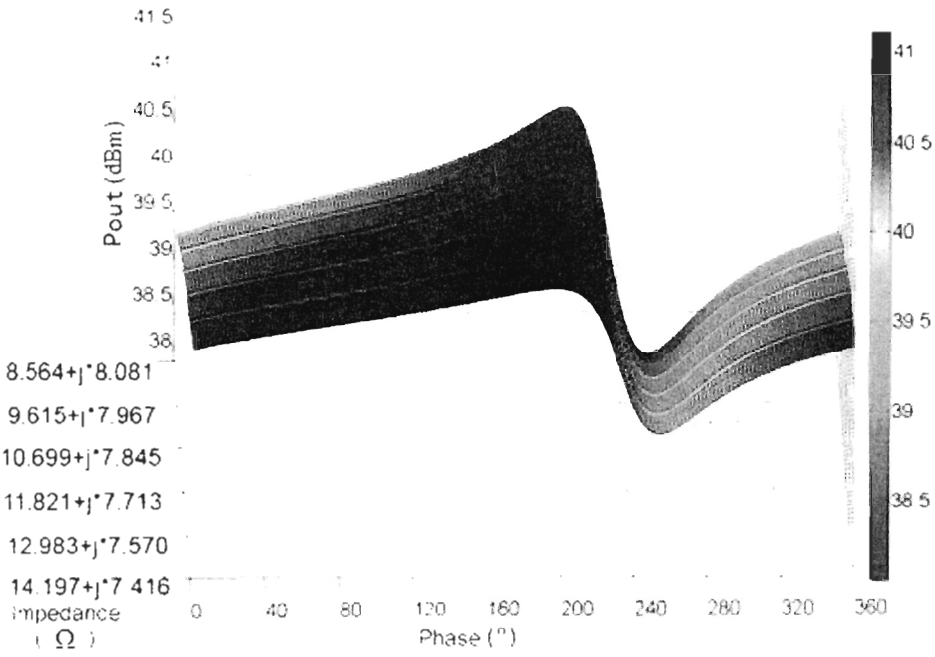


Figure 17 : Impedances chosen for analyzing the effect from the movement of impedance at fundamental frequency

In the simulation "One Tone, Load Harmonic Phase Sweep", the source impedance at fundamental frequency is fixed to 0.941∠-151.8°. Load impedances at the 3rd harmonic frequency, source impedance at the 2nd and 3rd harmonic frequencies are 50 Ω. Six different impedances as shown in Figure 17 are used one by one for the load impedance at 3.5GHz in this simulation. With these load impedances at fundamental frequency, the PAE and output power is simulated when the phase of the load impedance at the 2nd harmonic frequency is swept from -180° to 180° with the Γ of load impedance at the 2nd harmonic frequency equals to 1. Figure 18 shows the simulated PAE and output power versus the phase of the load impedance at the 2nd harmonic frequency with different load impedances at 3.5 GHz. From Figure 18 (a) and (b), we can see that the maximum PAE is increased and the maximum output power is reduced when the impedance changes from 14.20+j7.42 Ω to 8.56+j8.08 Ω.



(a)



(b)

Figure 18 : Simulated PAE (a) and output power (b) versus the phase of the load impedance at the 2nd harmonic frequency when the load impedance at fundamental frequency moves from 14.20+j7.42 Ω to 8.56+j8.08 Ω

By comparing the PAE and output power obtained in 3rd step by method no. 2 (PAE: 77.71% and P_{out}: 40.41 dBm) with the PAE and output power obtained in 3rd step by method no. 1 (PAE: 75.83%; P_{out}: 41.08 dBm), we can see that method no. 2 reduces the output power to increase the PAE.

As a fourth step, the source impedance at 3.5 GHz is fixed to 1.62-j12.53 Ω. The impedance of the load impedance at the 2nd harmonic frequency is fixed to $1.000\angle 144.0°$. The source impedances at the 2nd and 3rd harmonic frequencies are fixed to 50 Ω. Then, fix the Γ of load impedance at 10.5 GHz to 1, and change the phase of the load impedance at 10.5 GHz from -180° to 180° with 1° step. With each change of phase value, the load pull simulation at 3.5 GHz is operated. From each load pull simulation results, we choose the impedance at 3.5 GHz which offers the maximum PAE and record the corresponding PAE and output power.

The simulation result in Figure 19 shows that the PAE increased from 77.71% to 78.38% with 40.14 dBm output power by changing the load impedance at the 3rd harmonic frequency to $1.000\angle -172.0°$. The load impedance at fundamental frequency with 78.38% PAE and 40.14 dBm output power moves from 8.56+j8.08 Ω ($0.714 \angle 161.1°$) to 8.87+j8.17 Ω ($0.705\angle 160.9°$) when the load impedance at the 3rd harmonic frequency is tuned to $1.000\angle 172.0°$. The minimum PAE of 70.10% with 39.09 dBm output power is found when the phase is 0.0°.

By only controlling the load 2nd and 3rd harmonic frequencies, the PAE is increased from 66.36% to 78.38% while output power is maintained more than 40 dBm. By analyzing the effect of the phase of the load impedance at the 2nd and 3rd harmonic frequencies in the simulation results in Figure 16 and Figure 19, we can see that if there is 116.0° difference in phase of the load impedance at the 2nd harmonic frequency, the PAE could be reduced by 18.75%. If there is 172.0° difference in phase of the load impedance at the 3rd harmonic frequency, the PAE could be reduced by 8.28%. Thus, with method no. 2, we also can say

that the phases of load impedance at the 2nd and 3rd harmonic frequencies are important to provide a high PAE for an inverse class F PA.

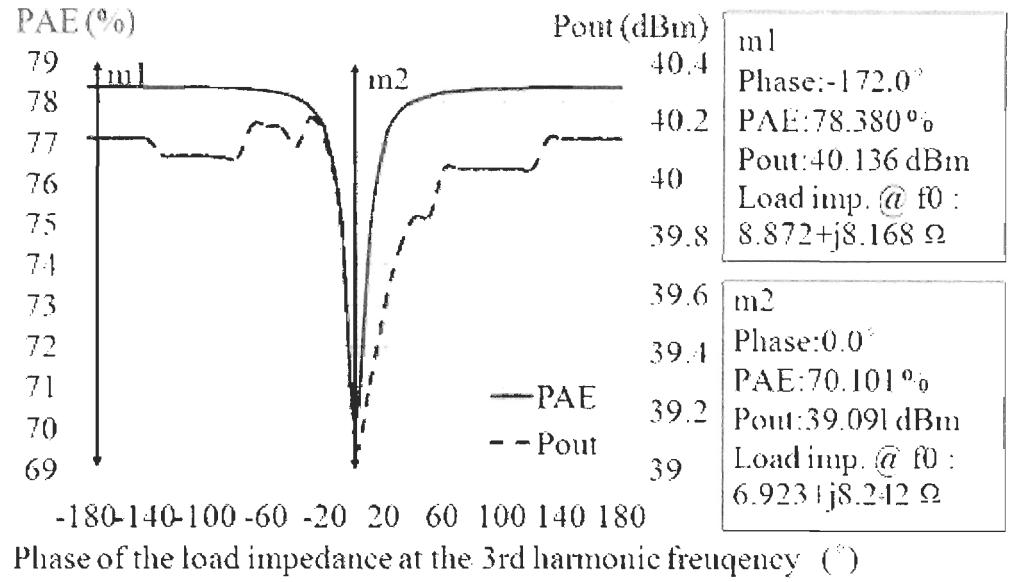


Figure 19 : Simulated PAE and output power versus the phase of the load impedance at the 3rd harmonic frequency by method no. 2

As a fifth step, the phase of the source impedance at the 2nd harmonic frequency is tuned. Source impedance at 3.5 GHz is fixed to $0.941\angle -151.8°$. The load impedances at the 2nd and 3rd harmonic frequencies are fixed to $1.000\angle 144.0°$ and $1.000\angle -172.0°$, respectively. The source impedances at the 2nd and 3rd harmonic frequencies are fixed to 50 Ω. The simulation result in Figure 20 shows that the maximum PAE can reach 82.26% with 40.00 dBm output power when the phase is -69.0° (m1 in Figure 20). However, by method no. 2, we also found that the PAE is sensitive to the phase of the source impedance at the 2nd harmonic frequency. It has the similar tendency as described in (Wu *et al.*, 2010b). If the phase is changed to -81.0°, the PAE could be reduced to 71.31% (m2 in Figure 20). The region with PAE fluctuation such as the region near -81° should be avoided. In this step, 0.0° is chosen for the phase of the source impedance at the 2nd harmonic frequency. At 0.0°, the PAE is 78.68% with 40.11 dBm output power (m3 in Figure 20).

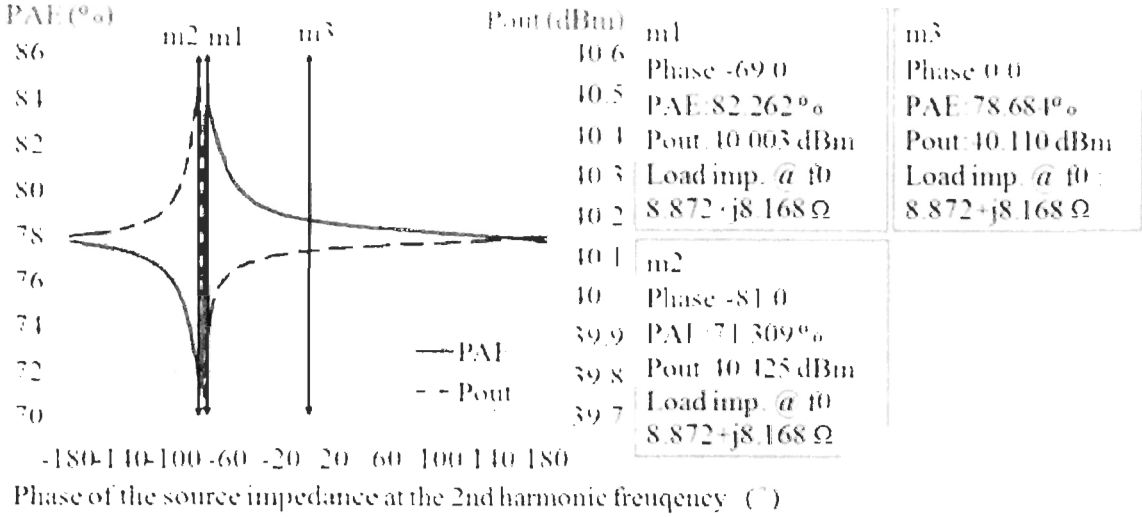


Figure 20 : Simulated PAE and output power versus the phase of the source impedance at the 2nd harmonic frequency by method no. 2

At last, the phase of the source impedance at the 3rd harmonic frequency is tuned. The source impedance at 3.5 GHz is fixed to $0.941\angle -151.8°$. The load impedances at the 2nd and 3rd harmonic frequencies are fixed to $1.000\angle 144.0°$ and $1.000\angle -172.0°$, respectively. The source impedance at the 2nd harmonic frequency is fixed to $1.000\angle 0.0°$. The simulation result in Figure 21 shows that the maximum PAE can reach 80.24% with 40.18 dBm output power when the phase of the source impedance at 3.5 GHz is 29.0° (m1 in Figure 21). However, by method no. 2, we also found that the PAE is sensitive to the phase of the source impedance at the 3rd harmonic frequency. If the phase is changed to 23.0°, the PAE could be reduced to 71.78% with 39.69 dBm output power (m2 in Figure 21). The region with PAE fluctuation such as the region near 23.0° should be avoided, so 180.0° is chosen for the phase of the source impedance at the 3rd harmonic frequency. At this impedance $1.000\angle 180.0°$, the PAE is 78.79% with 40.12 dBm output power (m3 in Figure 21).

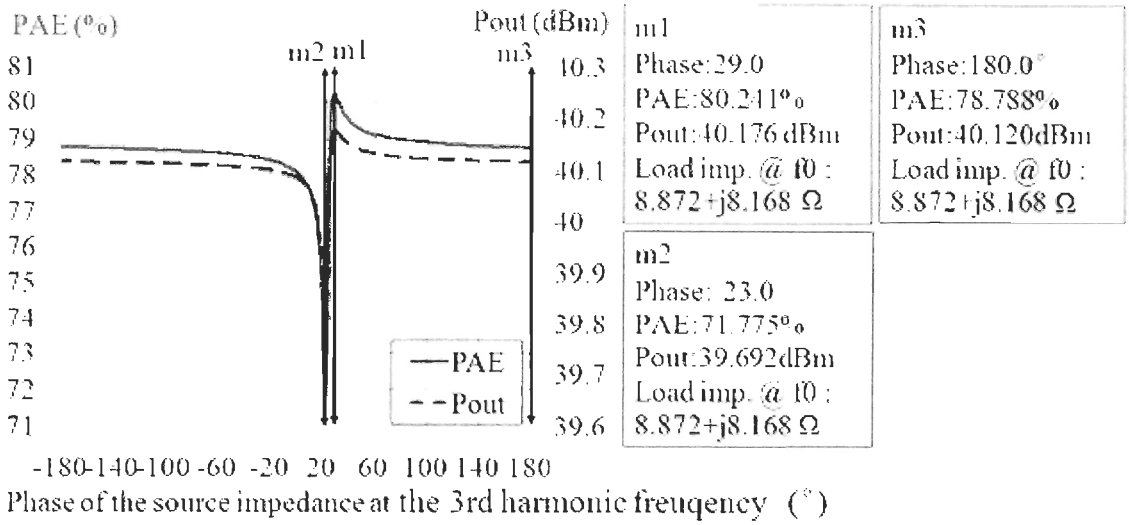


Figure 21 : Simulated PAE and output power versus the phase of the source impedance at the 3rd harmonic frequency by method no. 2

With this proposed characterization procedure, the chosen source and load impedances at the fundamental frequency, the 2nd harmonic and 3rd harmonic frequencies could offer 78.79% PAE with 40.12 dBm output power. Table 4 summarizes the procedure of the 1-tone characterization by the source & load pull simulation with method no. 2. From Table 4, we can see that the PAE is increased by 11.35% by tuning the load impedance at the 2nd harmonic. By tuning the load impedance at the 3rd harmonic, the PAE is increased by 0.67%.

Tuning the source impedance at the 2nd and 3rd harmonic does not improve the PAE significantly compared with tuning the load impedance at the 2nd and 3rd harmonic. With the chosen phases of the source impedances at the 2nd and 3rd harmonic frequency, only 0.41% PAE is increased in total. However, we found that the PAE is sensitive to the phase of the source impedance at the 2nd and 3rd harmonic frequencies. If the phase of the source impedance at the 2nd and 3rd harmonic frequencies is not well chosen, the PAE could be reduced by maximum 10.95%. Similar tendency is observed in the simulation results obtained in method no. 1 and in (Wu *et al.*, 2010a).

Thus, based on the characterization results obtained by the source & load pull simulation in ADS 2011.10 with CGH40010's large signal model, we can say that, besides of the 2nd and 3rd harmonics on the output side of the transistor, the 2nd and 3rd harmonics on the input side of the transistor are also important to achieve a high PAE inverse class F PA.

Table 4 : 1-tone characterization results obtained by the source & load pull simulation with method no. 2

	Frequency (GHz)	Source impedance	Load impedance	PAE (%)	P_{out} (dBm)
Step 1 Load pull @ 3.5 GHz	3.5	0.888∠-150.1°	0.566∠161.7°	65.23	40.33
	7	0∠0°	0∠0°		
	10.5	0∠0°	0∠0°		
Step 2 Source pull @ 3.5 GHz	3.5	0.941∠-151.8°	0.566∠161.7°	66.36	40.54
	7	0∠0°	0∠0°		
	10.5	0∠0°	0∠0°		
Step 3 Load pull @ 7 GHz	3.5	0.941∠-151.8°	0.714∠161.1°	77.71	40.41
	7	0∠0°	1.000∠144.0°		
	10.5	0∠0°	0∠0°		
Step 4 Load pull @ 10.5 GHz	3.5	0.941∠-151.8°	0.705∠160.9°	78.38	41.14
	7	0∠0°	1.000∠144.0°		
	10.5	0∠0°	1.000∠-172.0°		
Step 5 Source pull @ 7 GHz	3.5	0.941∠-151.8°	0.705∠160.9°	78.68	40.11
	7	1.000∠0.0°	1.000∠144.0°		
	10.5	0∠0°	1.000∠-172.0°		
Step 6 Source pull @ 10.5 GHz	3.5	0.941∠-151.8°	0.705∠160.9°	78.79	40.12
	7	1.000∠0.0°	1.000∠144.0°		
	10.5	1.000∠180.0°	1.000∠-172.0°		

2.4.1.3 Comparison of characterization results obtained by simulation method no. 1 and no. 2

By comparing the simulated characterization results obtained by method no. 1 with the characterization results obtained by method no. 2 in Table 5, we can see that method no. 2 provides 1.79% more PAE, but 1.01 dBm less output power than the method no. 1. Therefore, the procedure for the characterization by simulation method no. 2 could be used to achieve higher PAE but lower output power.

Table 5 : Comparison of 1-tone characterization results obtained by the source & load pull simulation with method no. 1 and by the source & load pull simulation with method no. 2

	1-tone characterization results obtained by simulation in ADS with method no. 1	**1-tone characterization results obtained by simulation in ADS with method no. 2**
Load imp. @ f_0	0.566∠161.7°	0.705∠160.9°
Load imp. @ $2f_0$	1.000∠-178.0°	1.000∠144.0°
Load imp. @ $3f_0$	1.000∠132.0°	1.000∠-172.0°
Source imp. @ f_0	0.941∠-151.8°	0.941∠-151.8°
Source imp. @ $2f_0$	1.000∠28.0°	1.000∠0.0°
Source imp. @ $3f_0$	1.000∠-135.0°	1.000∠180.0°
Final result	PAE: 77.00% P_{out}: 41.13 dBm	PAE: 78.79% P_{out}: 40.12 dBm

The chosen impedances at the fundamental, the 2nd and 3rd harmonic frequencies in the 1-tone characterization by the source & load simulation in ADS 2011.10 with method no. 1 and method no. 2 are plotted on the Smith chart as shown in Figure 22. For the chosen load impedances at 3.5 GHz obtained by two different methods, there are 0.139 and 0.8° differences in magnitude and phase, respectively. The chosen source impedances at 3.5 GHz are same. For the chosen impedances at the 2nd and 3rd harmonic frequencies, there is 28° to 56° differences in phase. We can see that with two different methods, the load impedance at the fundamental frequency and the impedances at the 2nd and 3rd harmonic frequencies are different. Consequently, the final characterization results are different.

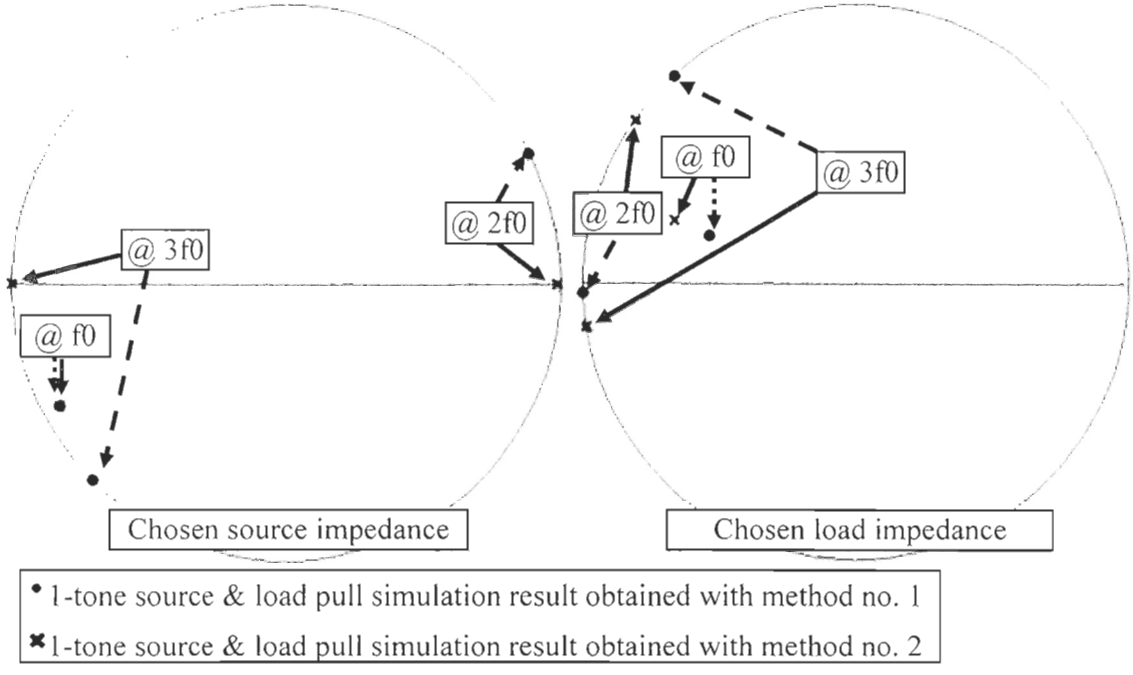


Figure 22 : Source (left) and load (right) impedances at the fundamental, 2nd and 3rd harmonic frequencies obtained by the source & load pull simulations in ADS2011.10 with method no. 1 and no. 2, where f_0 is 3.5 GHz.

In our case, we want to guarantee an output power of the inverse class F PA more than 40 dBm. Thus, for the Cree's CGH40010 transistor characterization by the source & load pull tuner system in the next section, the characterization procedure of method no. 1 is adopted.

2.4.2 Proposed method of 1-tone characterization of CGH40010 transistor by the multi-harmonic source & load pull tuner system

In this section, the method for characterizing the CGH40010 transistor by the multi-harmonic source & load pull tuner for a 1-tone signal at 3.5 GHz is proposed. The work in this section is published in the 2012 IEEE ARFTG microwave measurement conference (Gao *et al.*, 2012a). The setup of the source & load pull tuner system is shown in Figure 23.

The Cree's CGH40010 transistor with a lot number C118155 is a DUT in this setup as shown in Figure 23.

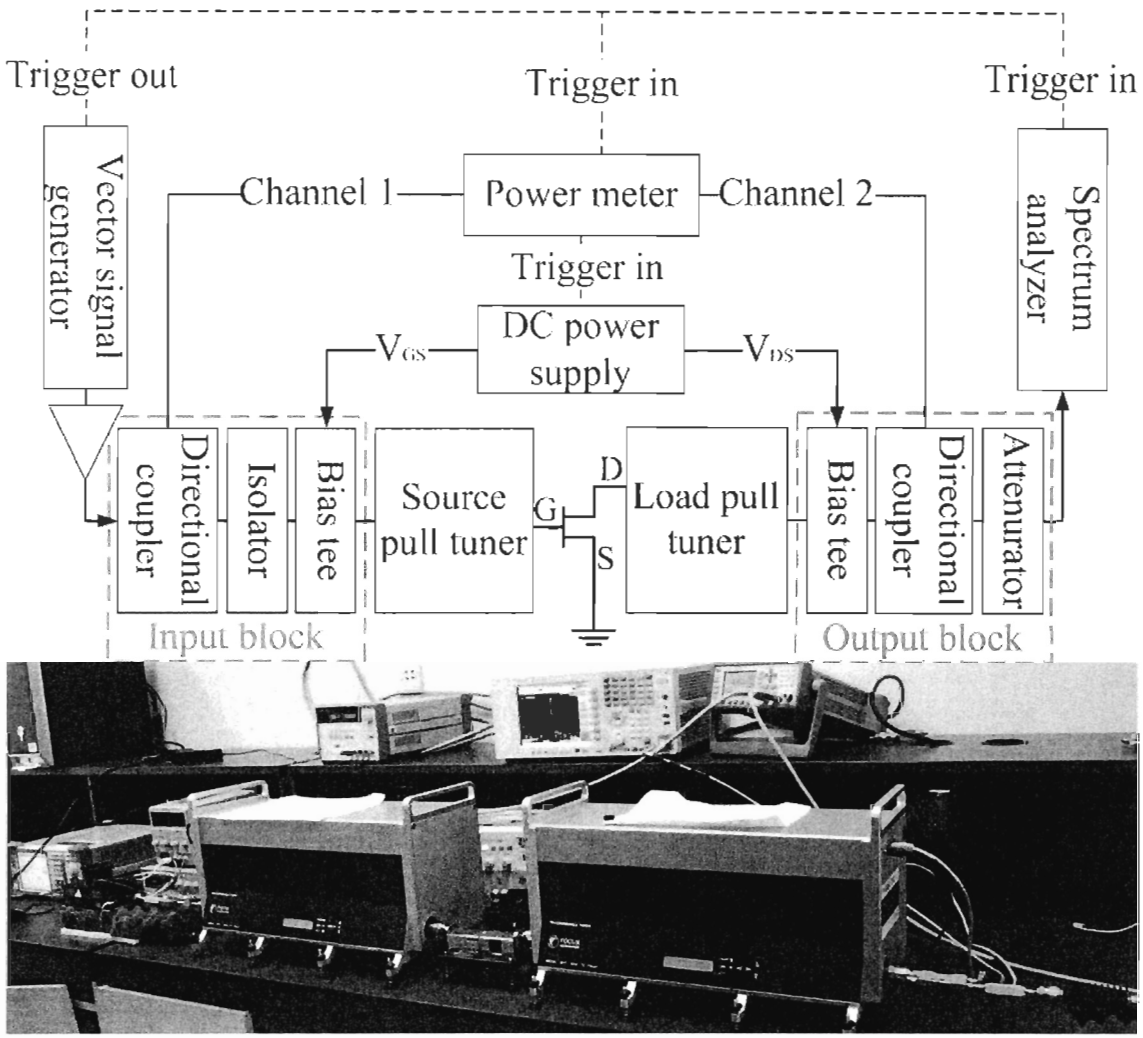


Figure 23 : Setup for the multi-harmonic source & load pull tuner system from Focus microwaves Inc.

Rohde & Schwarz SMBV100A vector signal generator, Agilent E3633A direct current (DC) power supply, N6705B DC power analyzer, Agilent MXA signal analyzer and Agilent N1912A P-series dual channel power meter are used in this system. These instruments are connected to a computer by the general purpose interface bus (GPIB) cables. In order to control the iMPT-1818-TC multi-harmonic source & load pull tuner and

obtain the measurement results from these instruments, such as input power, output power, V_{GS}, V_{DS}, etc., a corresponding software called "Load Pull Explorer" provided by Focus microwaves Inc. is installed in the computer. The input block in the source & load pull tuner system consists of a directional coupler, an isolator and a bias tee. The output block consists of a bias tee, a directional coupler and an attenuator. The accessories used in input and output block are chosen based on the research in (Gao *et al.*, 2012b).

For the inverse class F operation, the transistor is biased in class AB mode (Wu *et al.*, 2009). The I-V curve measured by the Focus microwaves' multi-harmonic source & load pull tuner system is shown in Figure 24. V_{GS}=-2.58V and V_{DS}=28V are chosen for the drain quiescent current of 200 mA, so that the transistor is biased in class AB mode. This bias condition in the source & load pull tuner system is same as the bias condition set in the source & load pull simulation in section 2.3.

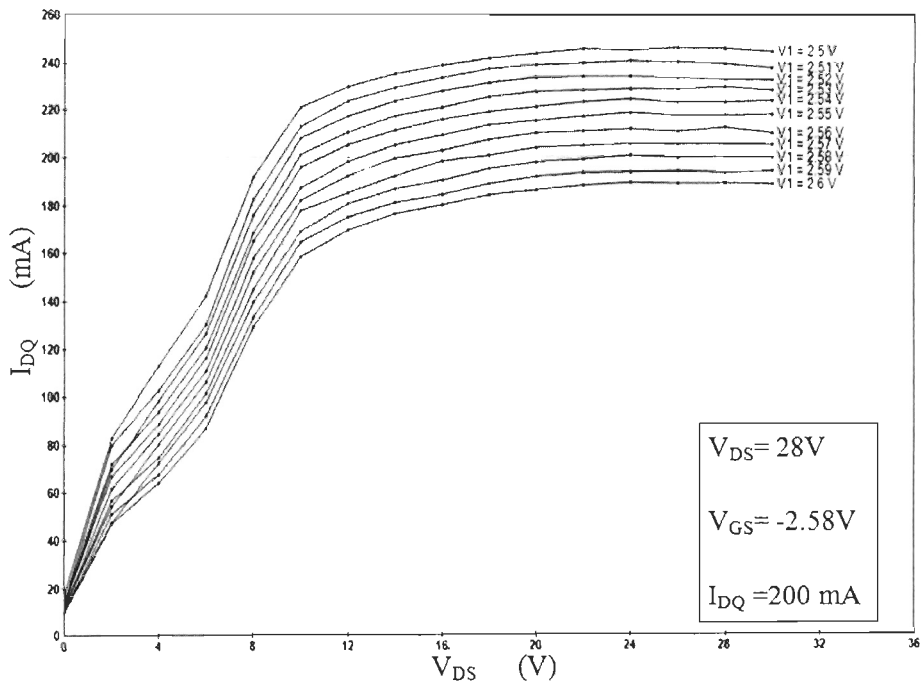


Figure 24 : Measured I-V curve for the Cree's CGH40010 transistor by the source & load pull tuner system

Before the characterization, the stability of the CGH40010 transistor should be analyzed. The stability circle can be determined from S-parameters of the transistor. To obtain the stability circle the transistor, the S-parameter of this transistor should be measured first. The setup for measuring the S-parameter of CGH40010 transistor is shown in Figure 25.

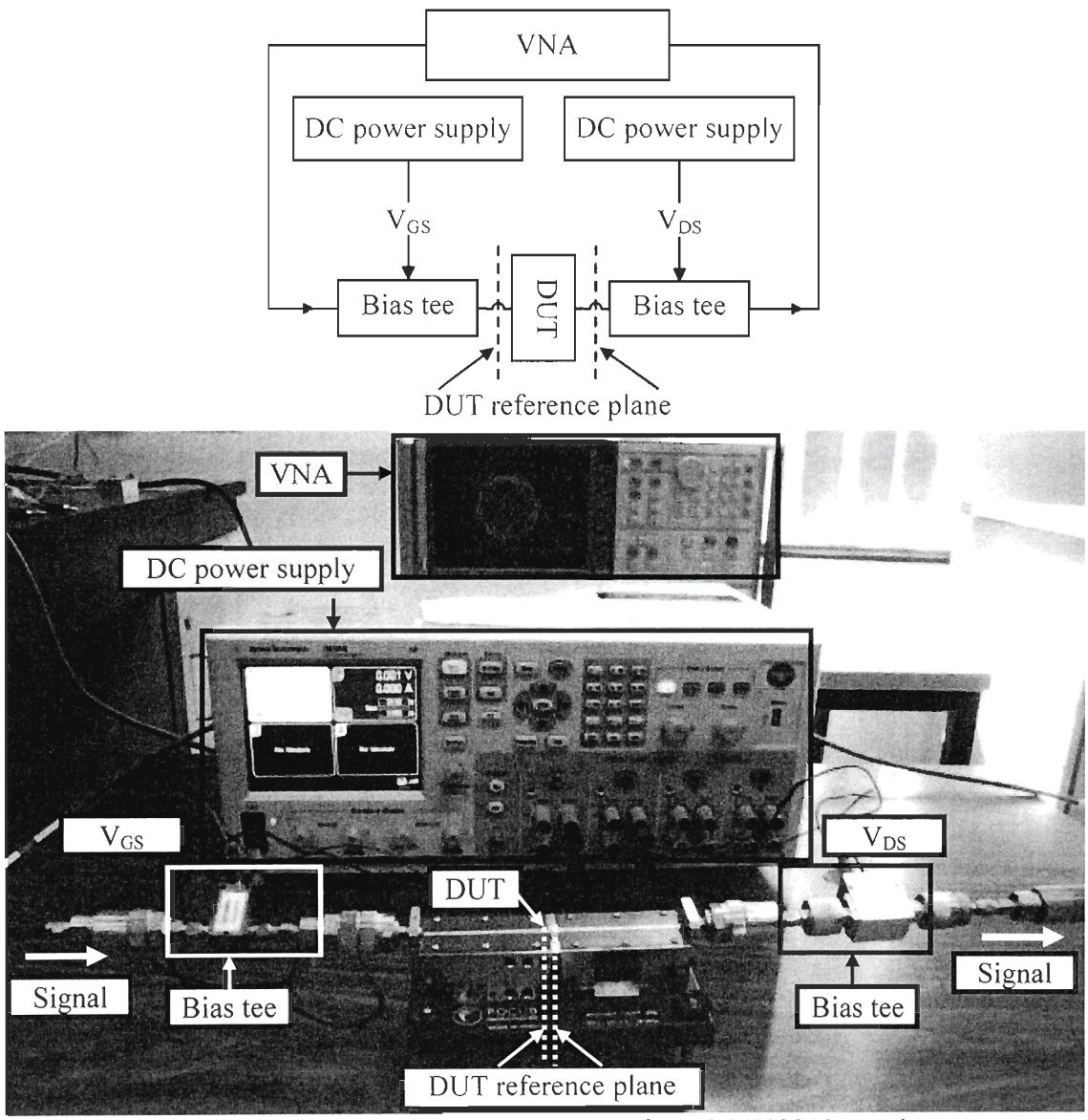


Figure 25 : Setup for measuring S-parameter of the CGH40010 transistor

Hewlett Packard 8719C Vector Network Analyzer (VNA) is used to measure S-parameter. Agilent N6705B DC power analyzer is used to provide DC power. Fairview SB18000 bias tee and Fairview SB4203 bias tee are added on the input and output side of the transistor to provide a path to transistor for V_{GS} and V_{DS}, respectively. The S-parameter is measured when CGH40010 transistor is biased at V_{DS}=28 V with 200 mA quiescent drain current as a class AB operation.

The measured S-parameter at the DUT reference plane at 3.5 GHz is compared with the S-parameter provided by the Cree Inc. (Cree Inc., 2012) in Table 6. From Table 6, we can see that there are 0.060 and 6.3° difference in magnitude and phase of S_{11}. For S_{22}, 0.093 and 8.4° difference in magnitude and phase. For S_{21}, 0.085 and 8.0° difference in magnitude and phase. For S_{12}, 0.008 and 34.4° difference in magnitude and phase. We assume that the difference between two S-parameters is caused by the difference between real transistor device and transistor model.

Table 6 : Comparison between measured S-parameter and the S-parameter provided by Cree Inc. for CGH40010 transistor at 3.5 GHz

	S_{11}	S_{21}	S_{12}	S_{22}
Measured S-parameter	0.827∠157.6°	2.940∠19.4°	0.016∠2.1°	0.553∠-166.1°
Cree's S-parameter	0.887∠151.3°	2.855∠27.4°	0.024∠-32.3°	0.460∠-174.5°

Figure 26 shows the comparison between the measured S-parameter and S-parameter provide by the Cree Inc. in the frequency range from 0.5 GHz to 6 GHz in Smith Chart. The tendency of the measured S-parameter of CGH40010 transistor is similar to the S-parameter provided by Cree Inc.

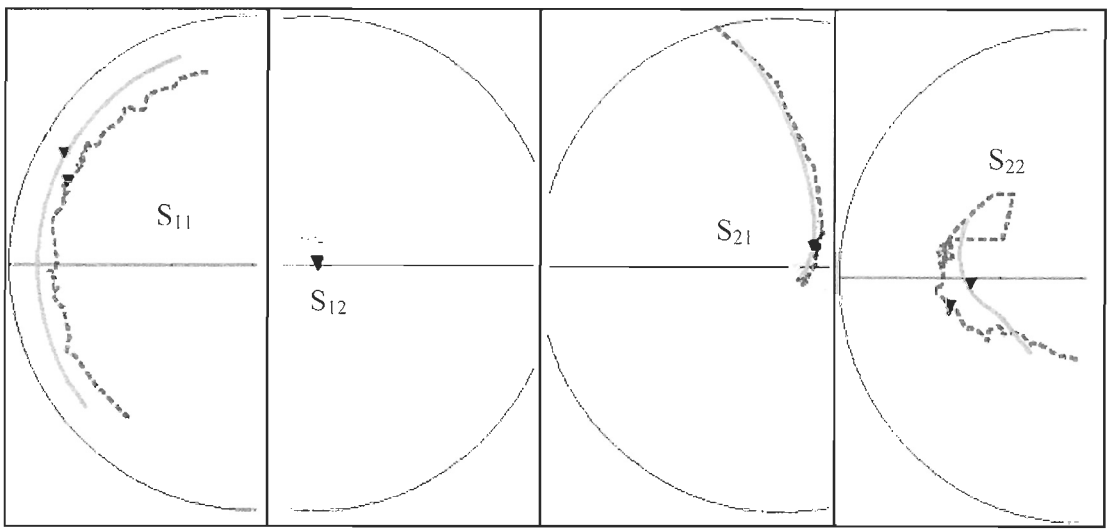


Figure 26 : Comparison between measured S-parameter of CGH40010 transistor (dotted line) and the small signal S-parameter of the CGH40010 transistor from Cree Inc. (solid line)

The measured S-parameter of the CGH40010 transistor is used to generate stability circle. The source and load stability circles at 3.5 GHz, 7 GHz and 10.5 GHz are shown in Figure 27. The source and load stability circles generated by the measured S-parameter of the CGH40010 transistor do not overlap with Smith chart, so the transistor is unconditionally stable (Gonzalez, 1996 : 219).

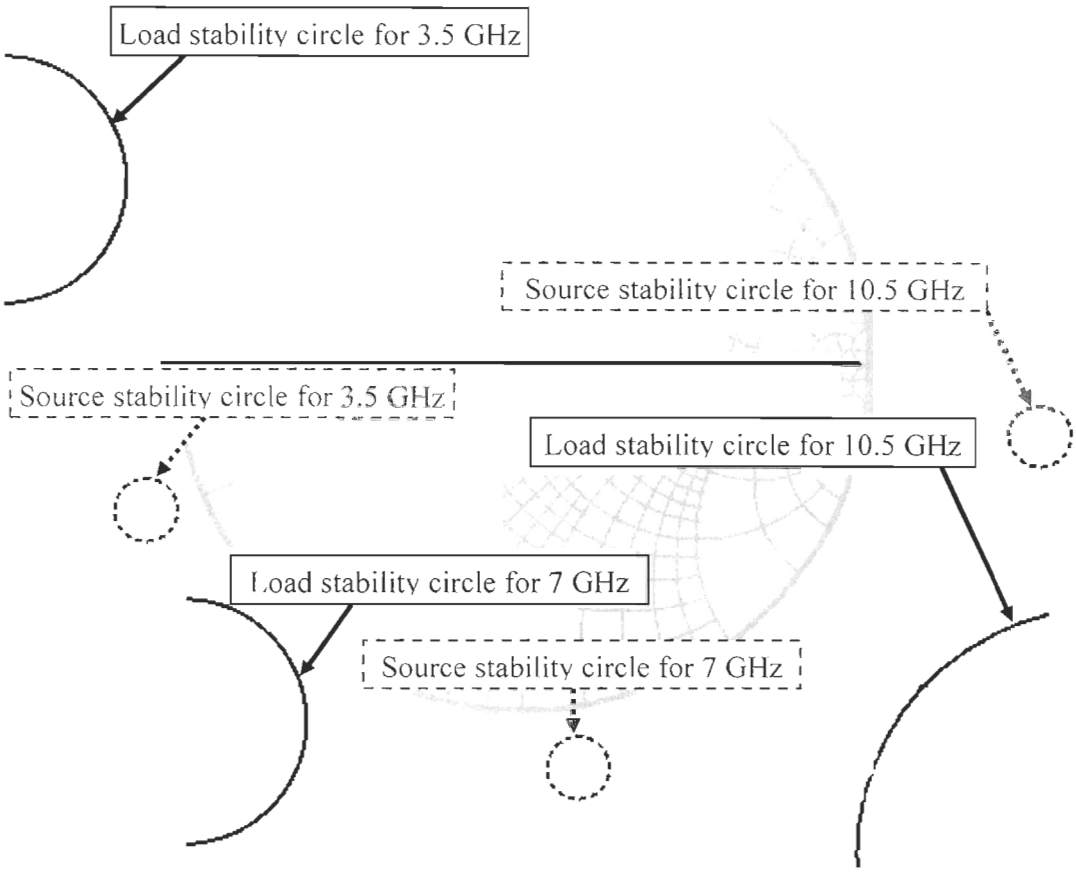
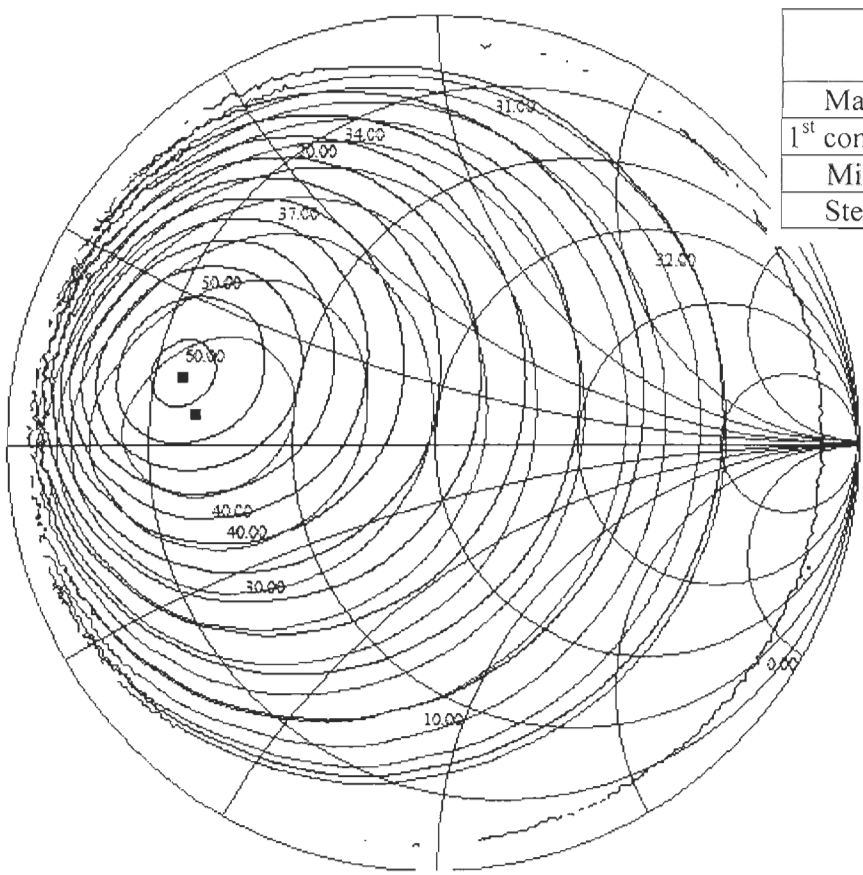


Figure 27 : Source (dotted line) and load (solid line) stability circles for 3.5 GHz, 7 GHz and 10.5 GHz by using the measured S-parameter of CGH40010 transistor

The objective of the characterization by Focus microwaves' multi-harmonic source & load pull tuner system is to obtain the maximum PAE when the output power is more than 40 dBm at 3.5 GHz with 25 dBm input power. When the transistor is characterized by the multi-harmonic source & load pull tuner system, V_{DS} and V_{GS} are fixed to 28V and -2.58V, respectively. The input power is fixed to 25 dBm. The characterization procedure used in this section is the same as the one for the characterization by the simulation method no. 1 described in section 2.3.1.1.

As a first step of the characterization by the multi-harmonic source & load pull tuner system, load pull characterization at 3.5 GHz is performed when the source impedance at

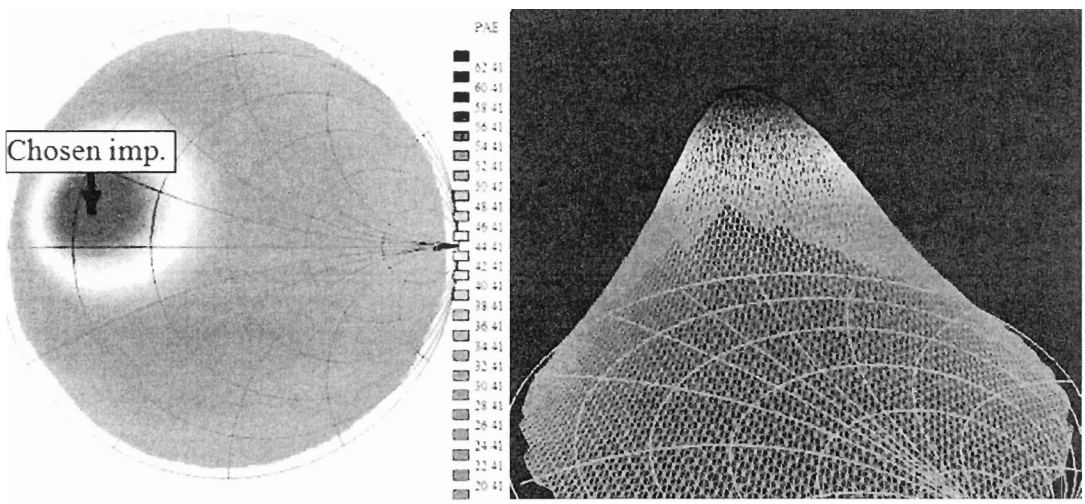
fundamental frequency is fixed to 3.18-j13.30 Ω (0.888∠-150.1°). The source & load impedances at the 2nd and 3rd harmonic frequencies are fixed to 50 Ω. The PAE and output power contour on Smith chart is shown in Figure 28. The maximum PAE obtained in the load pull characterization is 62.41% with 40.47 dBm output power when the load impedance at 3.5 GHz is 0.603∠165.5°. The maximum output power is 40.73 dBm with 59.14% PAE when the load impedance at 3.5 GHz is 0.559∠173.3°. In order to obtain 40 dBm output power and to have higher PAE, the maximum PAE impedance of 0.603∠ 165.5° is chosen for the next step.



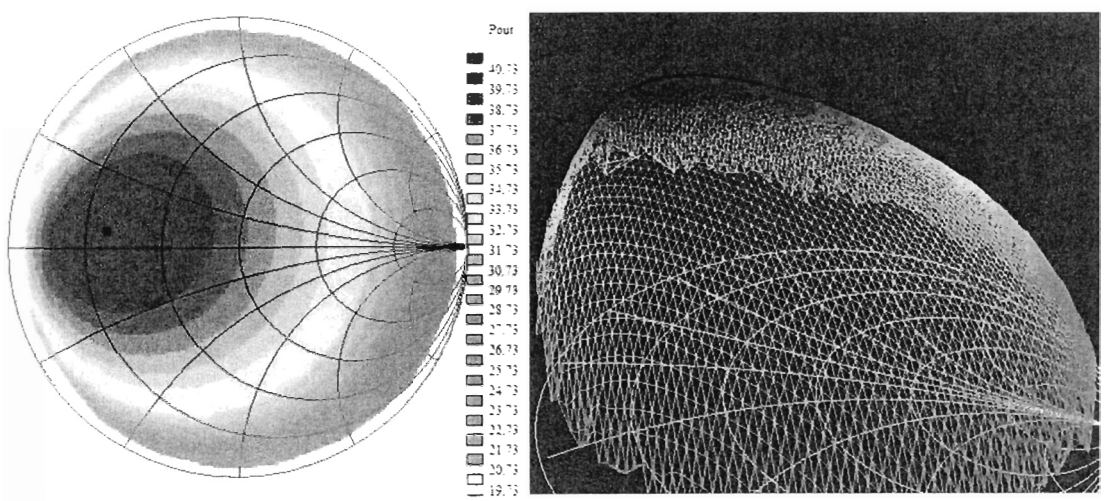
	PAE (%)	P_{out} (dBm)
Max	62.41	40.73
1st contour	57.41	39.73
Min	-1.14	22.19
Step	5.00	1.00

Figure 28 : Measured PAE and output power contour by the load pull tuner at 3.5 GHz

The measured PAE and output power contours in 3D are shown in Figure 29. From the 3D contour, we can see that the PAE is more sensitive to the impedance at 3.5 GHz than the output power.



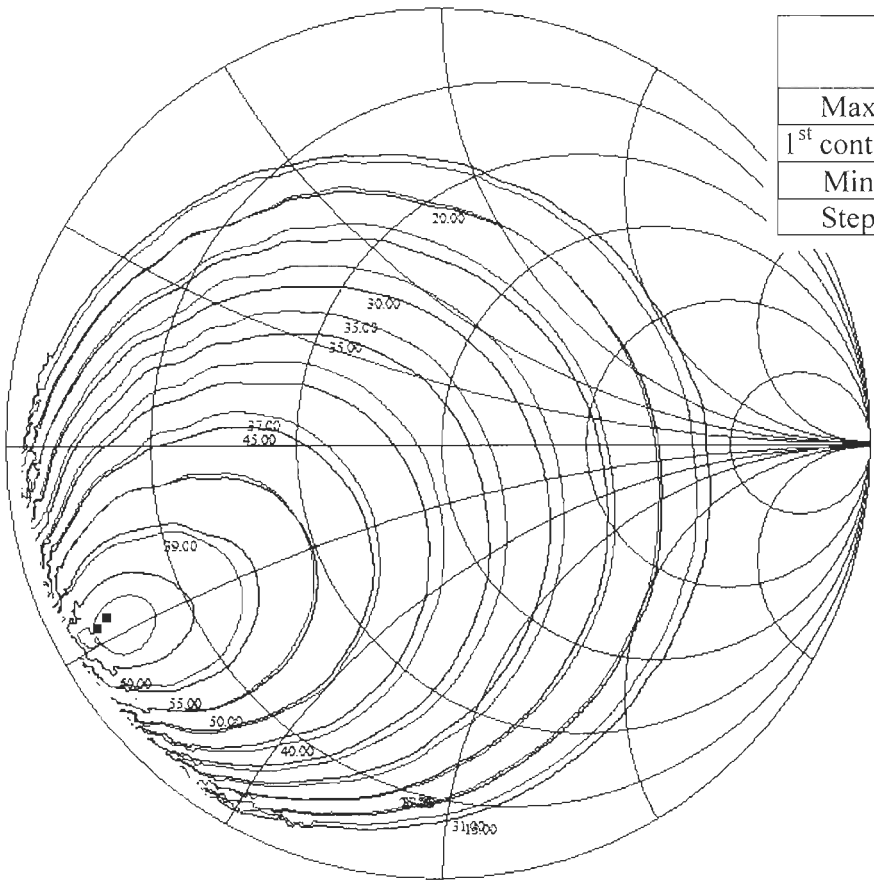
(a)



(b)

Figure 29 : Measured PAE (a) and output power contour (b) in 3D by the load pull tuner at 3.5 GHz

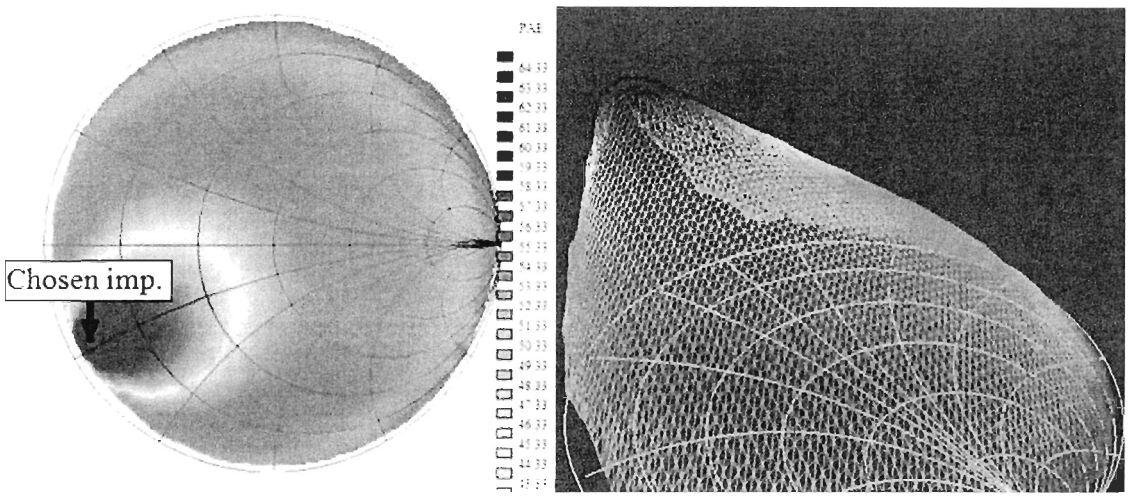
Then, as a second step, the source pull characterization is operated at the fundamental frequency when load impedance at fundamental frequency is fixed to 0.603∠165.5°. The source and load impedances at the 2nd and 3rd harmonic frequencies are fixed to 50 Ω. The source pull characterization result in Figure 30 shows that maximum PAE is 64.33% with 40.07 dBm output power when the source impedance at 3.5 GHz is 0.892∠-151.7°. The maximum output power is 40.32 dBm with 64.09% PAE when the source impedance is 0.861∠-152.5°. In order to have 40 dBm output power and a higher PAE, the maximum PAE impedance 0.892∠-151.7° is chosen for the further characterization.



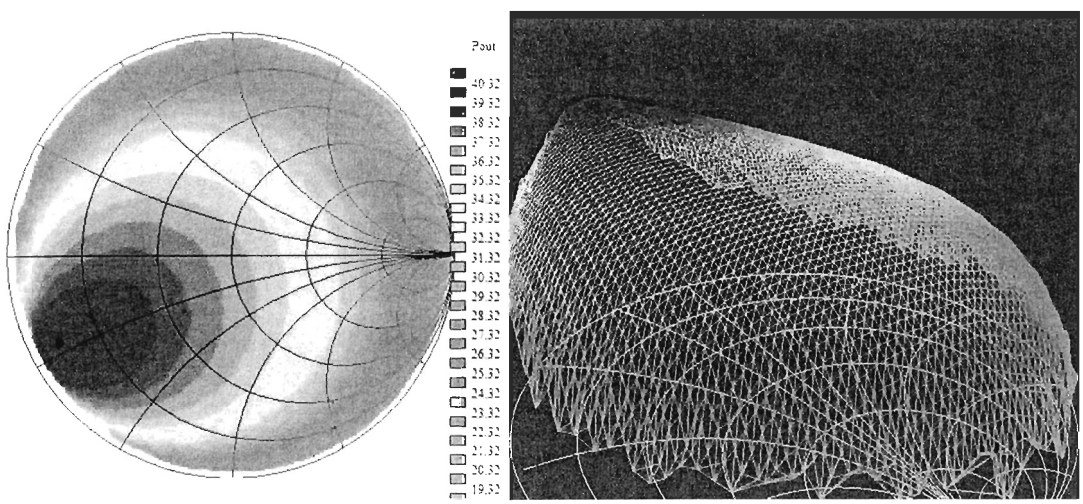
	PAE (%)	P_{out} (dBm)
Max	64.33	40.32
1st contour	59.33	39.32
Min	-9.47	13.07
Step	5.00	1.00

Figure 30 : Measured PAE and output power contour by the source pull tuner at 3.5 GHz

From the contours in 3D in Figure 31, we can also see that the PAE is more sensitive to the impedance variation at 3.5 GHz than output power.



(a)



(b)

Figure 31 : Measured PAE (a) and output power contour in 3D (b) by the source pull tuner at 3.5 GHz

As a third step, the load impedance at the 2nd harmonic frequency is tuned when the source and load impedances at fundamental frequency are fixed to the values which are

found in the previous steps (Source impedance at fundamental frequency: $0.892\angle$-151.7° and load impedance at fundamental frequency: $0.603\angle$165.5°). The load impedance at the 3rd harmonic frequency and source impedances at the 2nd and 3rd harmonic frequencies are fixed to 50 Ω.

Figure 32 shows the measured PAE contour in 3D by the multi-harmonic source & load tuner system at 7 GHz. PAE is increased to 68.48% with 40.06 dBm output power by tuning the load impedance at the 2nd harmonic frequency to $0.938\angle$146.1°. PAE is increased by 4.15% by tuning the load impedance at the 2nd harmonic frequency.

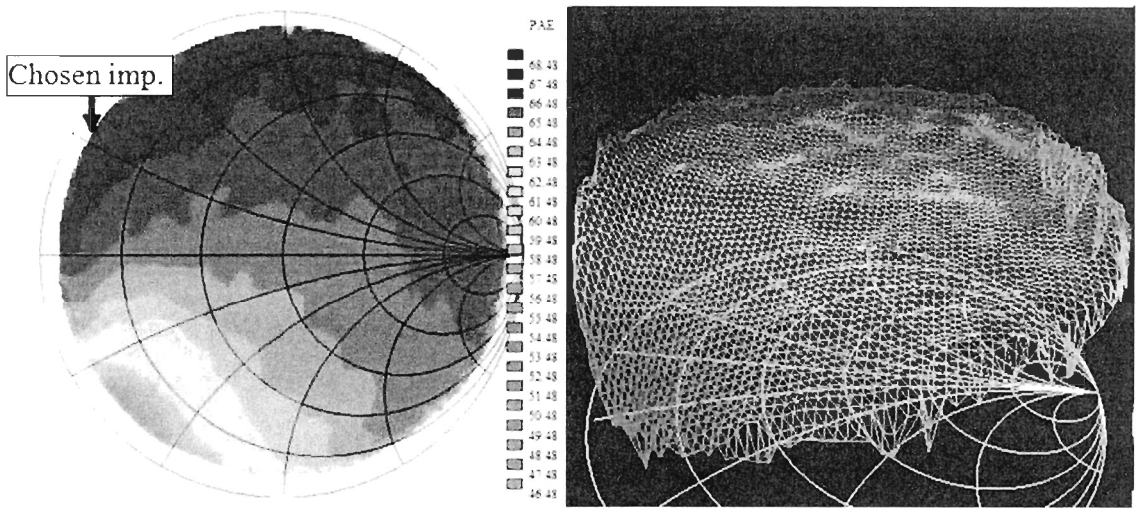


Figure 32 : Measured PAE contour in 3D by the load pull tuner at 7 GHz

In Figure 33, the measured PAE and output power versus the phase of the load impedance at 7 GHz when the Γ of load impedance at 7 GHz is maintained as close as possible to 1 is compared with the simulated PAE and output power versus the phase of the load impedance at 7 GHz obtained by method no. 1 in section 2.3.1.1. We can see that the tendency of measured output power and PAE is similar to the simulation results. If the phase of the load impedance at the 2nd harmonic frequency is -114.7°, the measured PAE is reduced to 57.10% with 38.81 dBm output power. Thus, by the tuner system, we can also say that the load impedance at the 2nd harmonic frequency is important for an inverse class F PA to achieve a high PAE. However, at the chosen impedance, the measured PAE and

output power is lower than the simulation. We assumed it can be caused by the difference between the real transistor device and the transistor model.

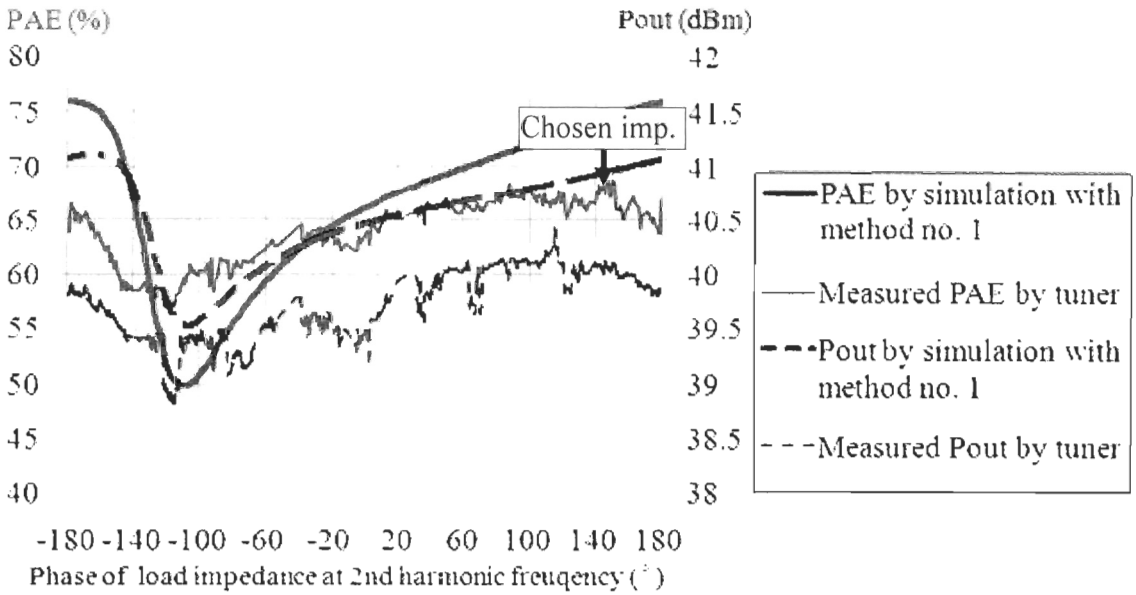


Figure 33 : PAE and output power versus the phase of the load impedance at 7 GHz by the tuner system and by the simulation method no. 1

As a fourth step, the load impedance at the 3rd harmonic frequency is tuned by the load pull tuner. The source and load impedance at the fundamental frequency is 0.892∠-151.7° and 0.603∠165.5°, respectively. The load impedance at the 2nd harmonic frequency is fixed to 0.938 ∠ 146.1° and the source impedances at the 2nd and 3rd harmonic frequencies are fixed to 50 Ω. The measured PAE contour in 3D in Figure 34 shows when the impedance at the 3rd harmonic frequency is 0.918 ∠ 42.6°, the PAE reaches the maximum as a 69.42% with 40.01 dBm output power. By considering the load impedance at the 3rd harmonic frequency, the PAE is increased by 0.94%.

In Figure 35, the measured PAE and output power versus the phase of the load impedance at 10.5 GHz when the Γ of load impedance at 10.5 GHz is maintained as close as possible to 1 are compared with the simulated PAE and output power versus the phase of the load impedance at 10.5 GHz obtained by the simulation method no. 1 in section 2.3.1.1.

If the phase of the load impedance at the 3rd harmonic frequency is 176.4°, the PAE is reduced to 57.26% with 39.02 dBm output power.

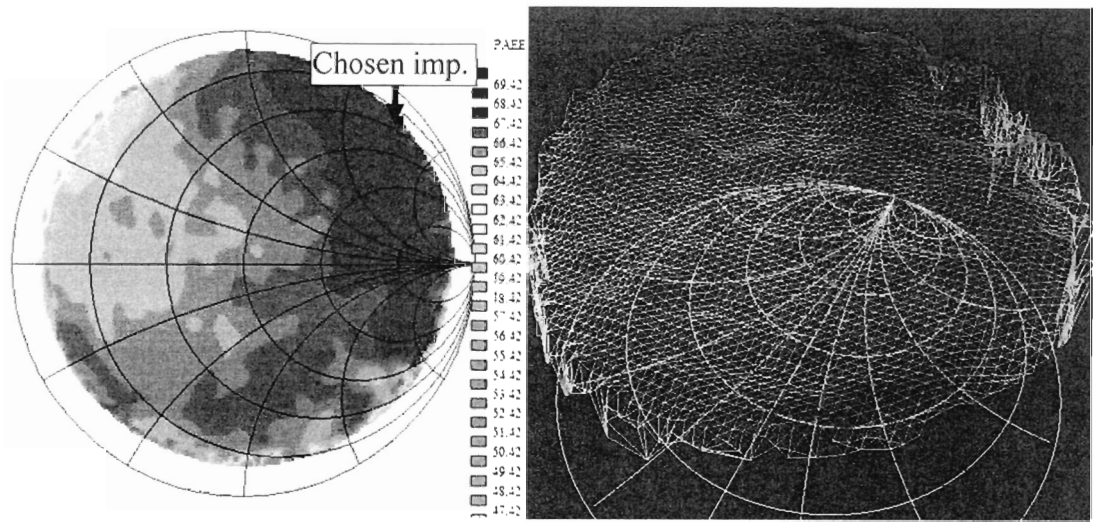


Figure 34 : Measured PAE contour in 3D by the load pull tuner at 10.5 GHz

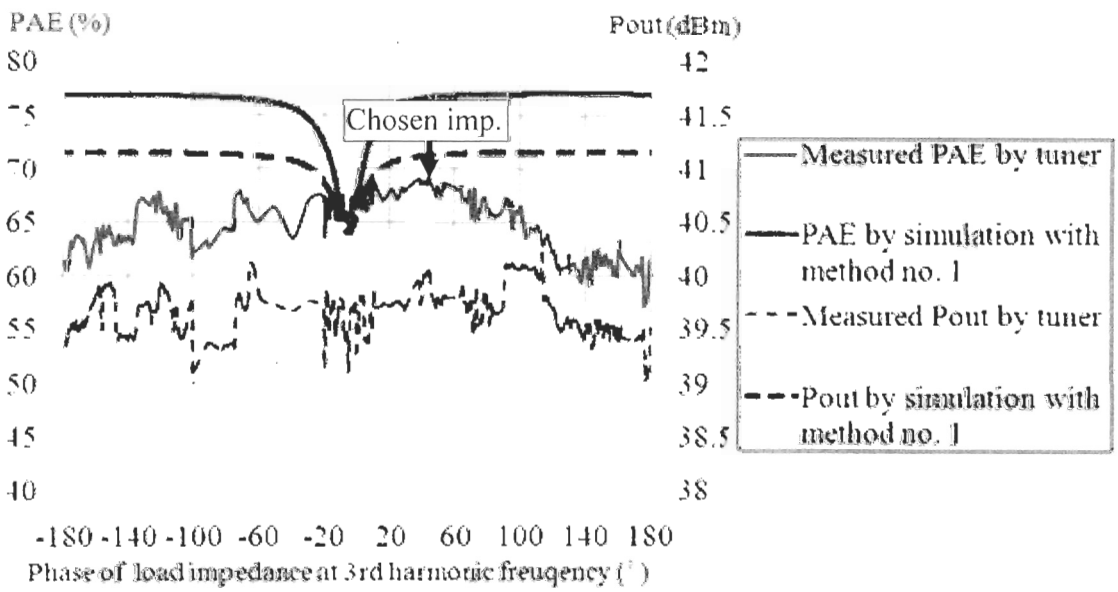


Figure 35 : PAE and output power versus the phase of the load impedance at 10.5 GHz by the tuner system and by the simulation method no. 1

In the 1-tone characterization by the source & load pull tuner system, the PAE is increased from 64.33% to 69.42% by only considering the load 2nd and 3rd harmonic while

output power is maintained more than 40 dBm. By analyzing the effect of the phase of the load impedance at the 2nd and 3rd harmonic frequencies based on the simulation results in Figure 33 and Figure 35, we can see that if there is 99.2° difference in the phase of the load impedance at the 2nd harmonic frequency, the PAE could be reduced by 11.38%. If there is 133.8° difference in the phase of the load impedance at the 3rd harmonic frequency, the PAE could be reduced by 12.16%. Thus, by the source & load pull tuner system, we can also prove that the phases of load impedance at the 2nd and 3rd harmonic frequencies are important to provide a high PAE for an inverse class F PA.

After tuning the load impedance at the 3rd harmonic frequency, the source impedance at the 2nd harmonic frequency is tuned. The source and load impedance at the fundamental frequency are fixed to 0.892 ∠ -151.7° and 0.603 ∠ 165.5°, respectively. The load impedances at the 2nd and 3rd harmonic frequencies are fixed to 0.938∠146.1° and 0.918∠ 42.6°, respectively. The source impedance at the 3rd harmonic frequency is fixed to 50 Ω. The measured PAE contour in 3D in Figure 36 shows that when source impedance at the 2nd harmonic frequency is 0.900∠-38.5°, the maximum PAE 73.08% can be obtained with 39.83 dBm output power. In this step, the PAE is increased by 3.66%.

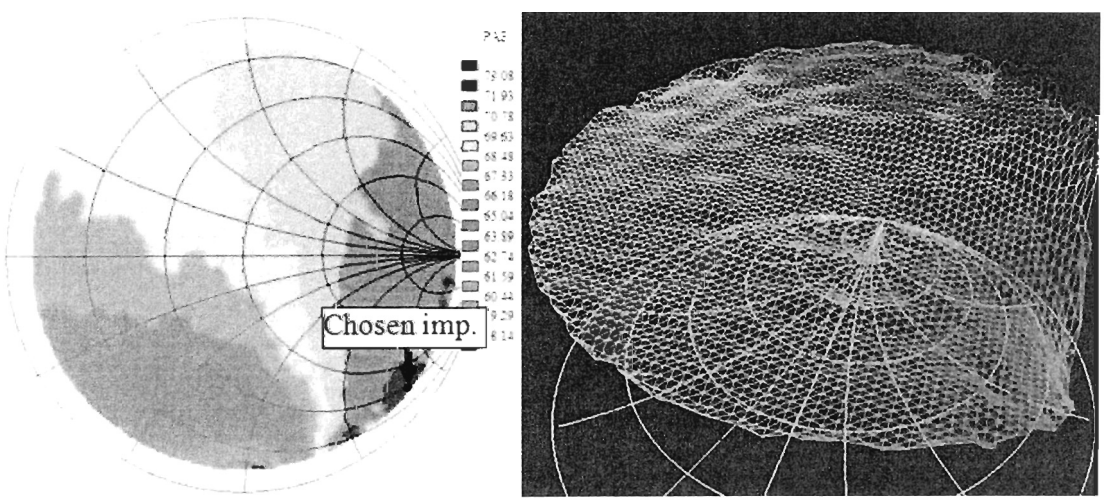


Figure 36 : Measured PAE contour in 3D by the source pull tuner at 7 GHz

The measured PAE and output power versus the phase of the source impedance at 7 GHz when the Γ of source impedance at 7 GHz is maintained as close as possible to 1 is compared with simulation results obtained by method no. 1 in section 2.3.1.1 as shown in Figure 37. We can see that the tendency of the measured output power and PAE is similar to the simulation results and the result obtained in (Wu *et al.*, 2010b). If the phase of the source impedance at the 2nd harmonic frequency is -88.0°, the PAE is reduced to 56.50% with 39.34 dBm output power.

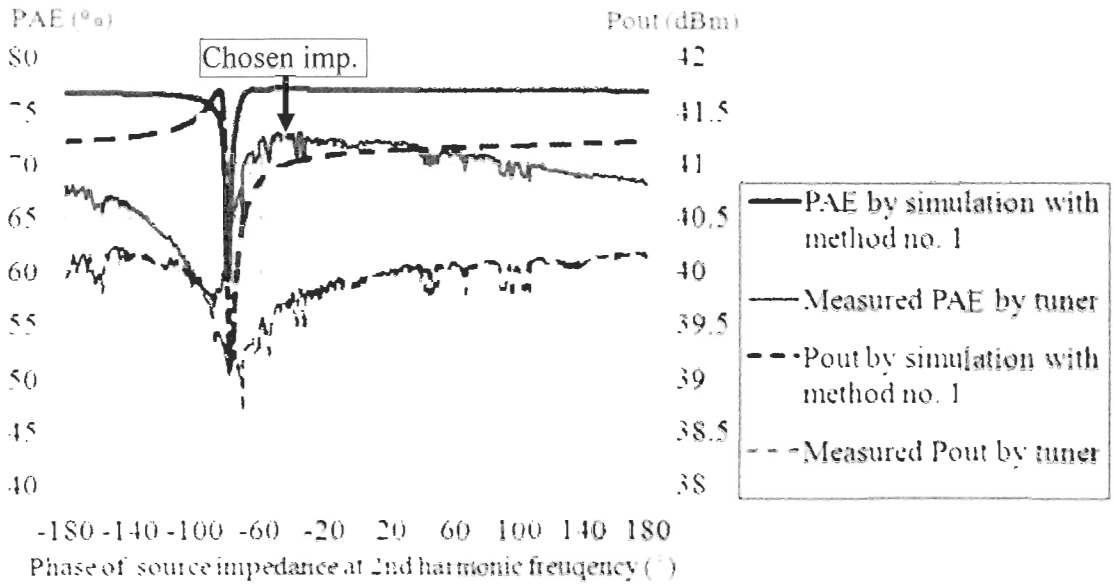


Figure 37 : PAE and output power versus the phase of the source impedance at 7 GHz by the tuner system and by the simulation with method no. 1

At last, the source impedance at the 3rd harmonic frequency is tuned. By tuning the source impedance at the 3rd harmonic frequency, the characterization result in Figure 38 shows that when the source impedance at the 3rd harmonic frequency is $0.880\angle$-68.6°, the maximum PAE 74.21% can be obtained with 39.92 dBm output power. In the last step, the PAE is increased the by 1.13% by tuning the source impedance at the 3rd harmonic frequency.

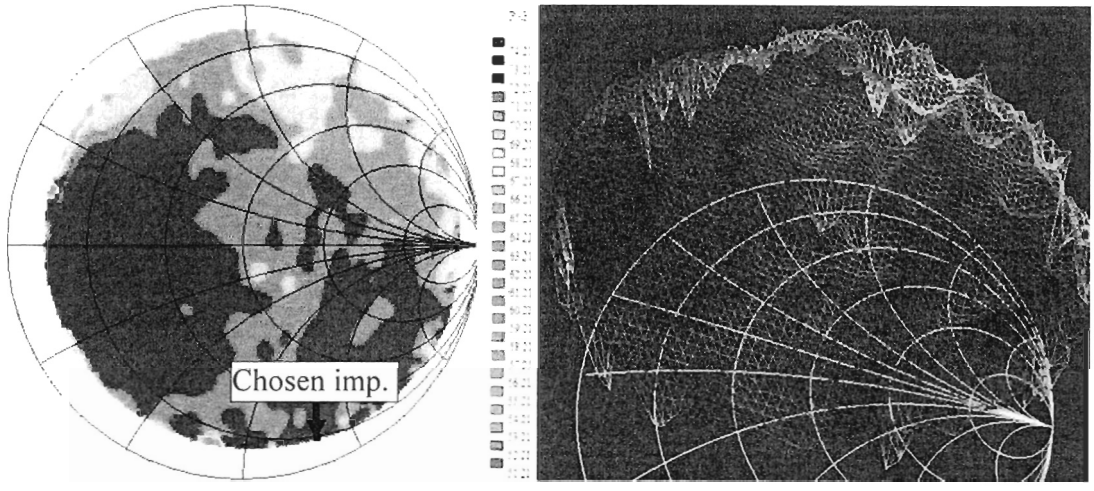


Figure 38 : Measured PAE contour in 3D by the source pull tuner at 10.5 GHz

The measured PAE and output power versus the phase of the source impedance at 10.5 GHz when the Γ of source impedance at 10.5 GHz is maintained as close as possible to 1 is compared with simulation results obtained by method no. 1 in section 2.3.1.1 as shown in Figure 39. If the phase of the source impedance at the 3rd harmonic frequency is -155.0°, the PAE is reduced to 61.22% with 38.13 dBm output power.

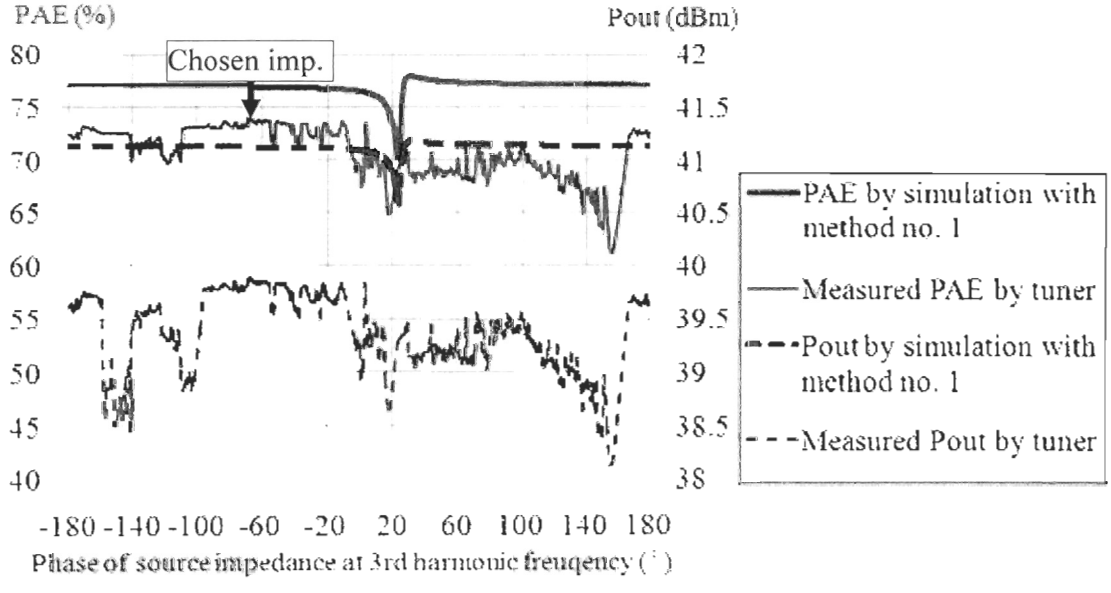


Figure 39 : PAE and output power versus the phase of the source impedance at 10.5 GHz by the tuner system by the simulation with method no. 1

By using the multi-harmonic source & load pull tuner from Focus microwaves Inc., the chosen source and load impedances at the fundamental frequency, the 2nd harmonic and 3rd harmonic frequencies could offer 74.21% PAE and 39.92 dBm output power.

Table 7 summarizes the procedure of 1-tone characterization by the source & load pull tuner system. The PAE is increased by 4.15% and 0.95% by tuning the load impedance at the 2nd and 3rd harmonics, respectively. By tuning the source impedance at the 2nd and 3rd harmonics, the PAE is increased by 3.66% and 1.13%, respectively. By Focus microwaves' multi-harmonic source & load pull tuner, we also proved that the PAE is sensitive to the source impedances at the 2nd and 3rd harmonic frequencies.

Table 7 : 1-tone characterization results obtained by the multi-harmonic source & load pull tuner system

	Frequency (GHz)	Source impedance	Load impedance	PAE (%)	P_{out} (dBm)
Step 1 Load pull @ 3.5 GHz	3.5	0.888∠-150.1°	0.603∠165.5°	62.41	40.47
	7	0∠0°	0∠0°		
	10.5	0∠0°	0∠0°		
Step 2 Source pull @ 3.5 GHz	3.5	0.892∠-151.7°	0.603∠165.5°	64.33	40.07
	7	0∠0°	0∠0°		
	10.5	0∠0°	0∠0°		
Step 3 Load pull @ 7 GHz	3.5	0.892∠-151.7°	0.603∠165.5°	68.48	40.06
	7	0∠0°	0.938∠146.1°		
	10.5	0∠0°	0∠0°		
Step 4 Load pull @ 10.5 GHz	3.5	0.892∠-151.7°	0.603∠165.5°	69.42	40.01
	7	0∠0°	0.938∠146.1°		
	10.5	0∠0°	0.918∠42.6°		
Step 5 Source pull @ 7 GHz	3.5	0.892∠-151.7°	0.603∠165.5°	73.08	39.83
	7	0.900∠-38.5°	0.938∠146.1°		
	10.5	0∠0°	0.918∠42.6°		
Step 6 Source pull @ 10.5 GHz	3.5	0.892∠-151.7°	0.603∠165.5°	74.21	39.92
	7	0.900∠-38.5°	0.938∠146.1°		
	10.5	0.880∠-68.6°	0.918∠42.6°		

2.4.3 Comparison between the 1-tone characterization results

The characterization results obtained by the source & load pull simulation with method no. 1 and by the multi-harmonic source & load pull tuner system is compared because the same procedure is adopted in both characterizations in Table 8.

Table 8 : Comparison of 1-tone characterization results obtained by the source & load pull simulation with method no. 1 and by the source & load pull tuner system, where f_0 is 3.5 GHz

	1-tone characterization results obtained by the simulation with method no. 1		**1-tone characterization results obtained by the source & load pull tuner system**	
Step 1 Load pull @ f_0	Load imp. @ f_0: 0.566∠161.7°	PAE: 65.23% P_{out}: 40.33 dBm	Load imp. @ f_0: 0.603∠165.5°	PAE: 62.41% P_{out}: 40.47 dBm
Step 2 Source pull @ f_0	Source imp. @ f_0: 0.941∠-151.8°	PAE: 66.36% P_{out}: 40.54 dBm	Source imp. @ f_0: 0.892∠-151.7°	PAE: 64.33% P_{out}: 40.07 dBm
Step 3 Load pull @ $2f_0$	Load imp. @ $2f_0$: 1.000∠-178.0°	PAE: 75.83% P_{out}: 41.08 dBm	Load imp. @ $2f_0$: 0.938∠146.1°	PAE: 68.48% P_{out}: 40.06 dBm
Step 4 Load pull @ $3f_0$	Load imp. @ $3f_0$: 1.000∠132.0°	PAE: 76.93% P_{out}: 41.15 dBm	Load imp. @ $3f_0$: 0.918∠42.6°	PAE: 69.42% P_{out}: 40.01 dBm
Step 5 Source pull @ $2f_0$	Source imp. @ $2f_0$: 1.000 ∠28.0°	PAE: 76.93% P_{out}: 41.12 dBm	Source imp. @ $2f_0$: 0.900∠-38.5°	PAE: 73.08% P_{out}: 39.83 dBm
Step 6 Source pull @ $3f_0$	Source imp. @ $3f_0$: 1.000∠-135.0°	PAE: 77.00% P_{out}: 41.13 dBm	Source imp. @ $3f_0$: 0.880∠-68.6°	PAE: 74.21% P_{out}: 39.92 dBm

From the comparison, we can see that in the first step, for the chosen load impedance at 3.5 GHz for the maximum PAE, there is 0.037 difference in magnitude and 3.7° difference in phase. The simulation predicts 2.82% more PAE than the tuner system.

In the second step, there is 0.049 difference in magnitude and 0.14° difference in the phase of the chosen source impedance at 3.5 GHz. The simulation predicts 2.03% more PAE than the tuner system.

In the third step, for the chosen load impedance at 7 GHz for the maximum PAE, there is 35.9° difference in phase between the results obtained by the simulation and the tuner system. The simulation result shows that the PAE could be increased by 9.47% by controlling the load 2^{nd} harmonic, while the PAE is only increased by 4.15% in the characterization by the source & load pull tuner system.

In the fourth step, for the chosen load impedance at 10.5 GHz for the maximum PAE, there is 89.4° difference in phase between the results obtained by the simulation and the tuner system. The simulation result shows that the PAE could be increased by 1.09% by controlling the load impedance at 3^{rd} harmonic, while the PAE is increased by 0.95% in the characterization by the source & load pull tuner system.

In the fifth step, for the source impedance at 2^{nd} harmonic, the source impedances at 7 GHz obtained by the source pull simulation and the source & load pull tuner system have 66.5° difference in phase. The simulation result shows that the PAE is increased by 0.15% by tuning the source impedance at the 2^{nd} harmonic frequency, while the PAE is increased by 3.66% in the characterization by the source & load pull tuner system.

In the sixth step, for the source impedance at 3^{rd} harmonic, the source impedances at 10.5 GHz obtained by the source pull simulation and source & load pull tuner system have 66.4° difference in phase. The simulation result shows that the PAE is increased by 0.60% by tuning the source impedance at the 3^{rd} harmonic, while the PAE is increased by 1.13% in the characterization by the source & load pull tuner system.

The final result predicted by simulation has 3.47% difference in PAE and 1.13 dBm difference in output power from the results obtained by the multi-harmonic source & load pull tuner system. We assumed that the differences between the results obtained by two

different methods can be caused by the difference between the real transistor device and the transistor model.

The chosen impedances at the fundamental frequency, the 2nd and 3rd harmonic frequencies in the 1-tone characterizations by the tuner system and by the simulation method no. 1 and method no. 2 are plotted on the Smith chart as shown in Figure 40.

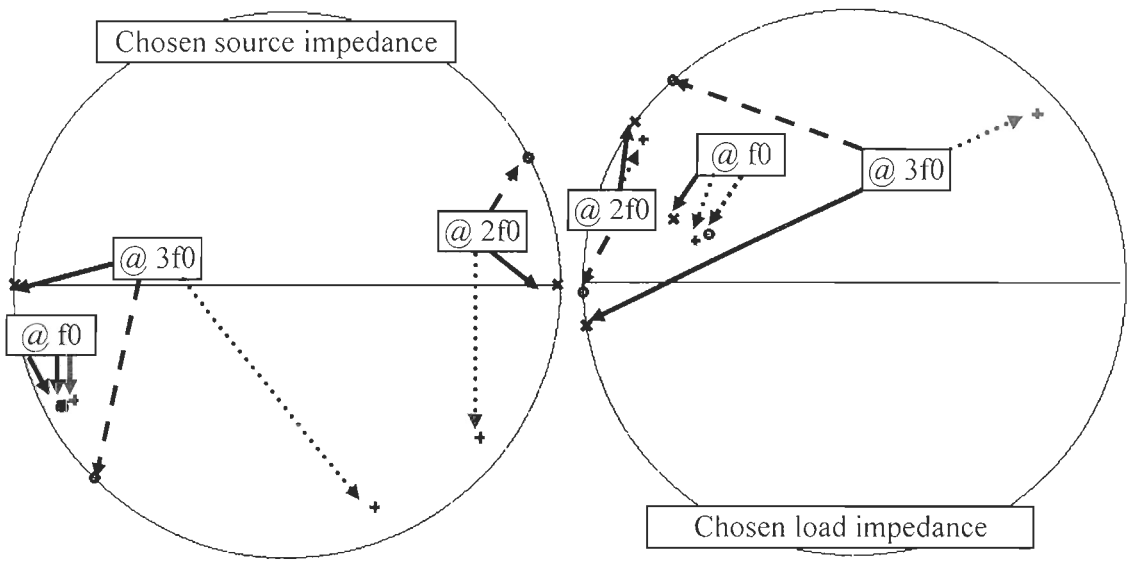


Figure 40 : Comparison between the characterization results obtained by the source & load pull simulation with method no. 1 (point) and with method no. 2 (x) and by the source & load pull tuner system (cross), where f_0 is 3.5 GHz

From the impedances on the Smith chart, we can see that the chosen source and load impedances at fundamental frequency in different characterizations are similar, but the impedances at the 2nd and 3rd harmonic frequencies in different characterizations are different from each other. We assume that these differences are caused by the differences between the transistor model and the real transistor device when the transistor is under large signal excitation. To evaluate these characterization results, the inverse class F PAs

should be designed and fabricated by using these impedances obtained in these characterizations.

2.5 PROPOSED METHOD OF LTE CHARACTERIZATION OF CGH40010 TRANSISTOR BY MULTI-HARMONIC SOURCE & LOAD PULL TUNER SYSTEM

In this part, in order to achieve a first-pass design for the inverse class F PA used in the LTE base station in Europe, the method for characterizing the CGH40010 transistor by the multi-harmonic source & load pull tuner with a LTE signal is proposed. The CGH40010 transistor with lot number C118155 is used as a DUT in the multi-harmonic source & load pull tuner system. For the LTE base station in Europe, the 3.5 GHz is allocated (Motorola Inc., 2012). The 3.5 GHz is the center frequency of No. 42 evolved universal terrestrial access (E-UTRA) down link operating band. The duplexing mode for the downlink direction is time division duplex (TDD) (3GPP org., 2012 d : 39). To generate this LTE signal, Rohde & Schwarz SMBV100A vector signal generator is used and configured as shown in Figure 41. For testing the signal in base station, the test model E-TM 1.1 with 10 MHz bandwidth is used (3GPP org., 2012 d : 47). The center frequency is set to 3.5 GHz. The duplexing mode for downlink direction is fixed to TDD. The parameters of the used LTE signal are summarized in Table 9.

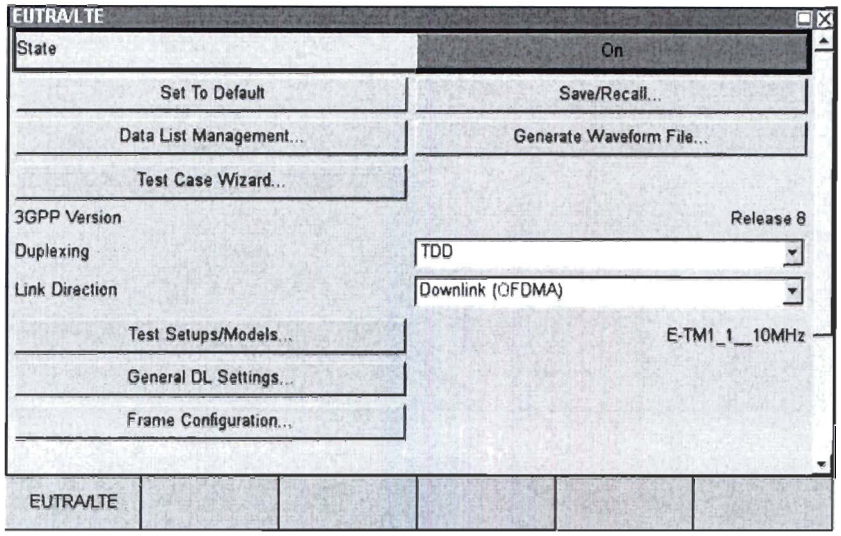


Figure 41 : Setup of Rohde & Schwarz SMBV100A vector signal generator for a LTE signal at 3.5 GHz with 10 MHz bandwidth

Table 9 : Parameters of the LTE signal generated by Rohde & Schwarz SMBV100A vector signal generator

Parameters of LTE signal	
Base station region	Europe
Frequency (GHz)	3.5
Bandwidth (MHz)	10
Duplexing mode	TDD
Link direction	Downlink
Test model	E-TM 1.1

For analyzing the LTE signal, the Agilent N9020A MXA signal analyzer with N9082A LTE TDD measurement application is used. Based on the LTE TDD measurement application measurement guide (Agilent technologies Inc., 2012), the pre-defined mask for E-TM 1.1 with 10 MHz bandwidth is used to measure the LTE signal as shown in Figure 42.

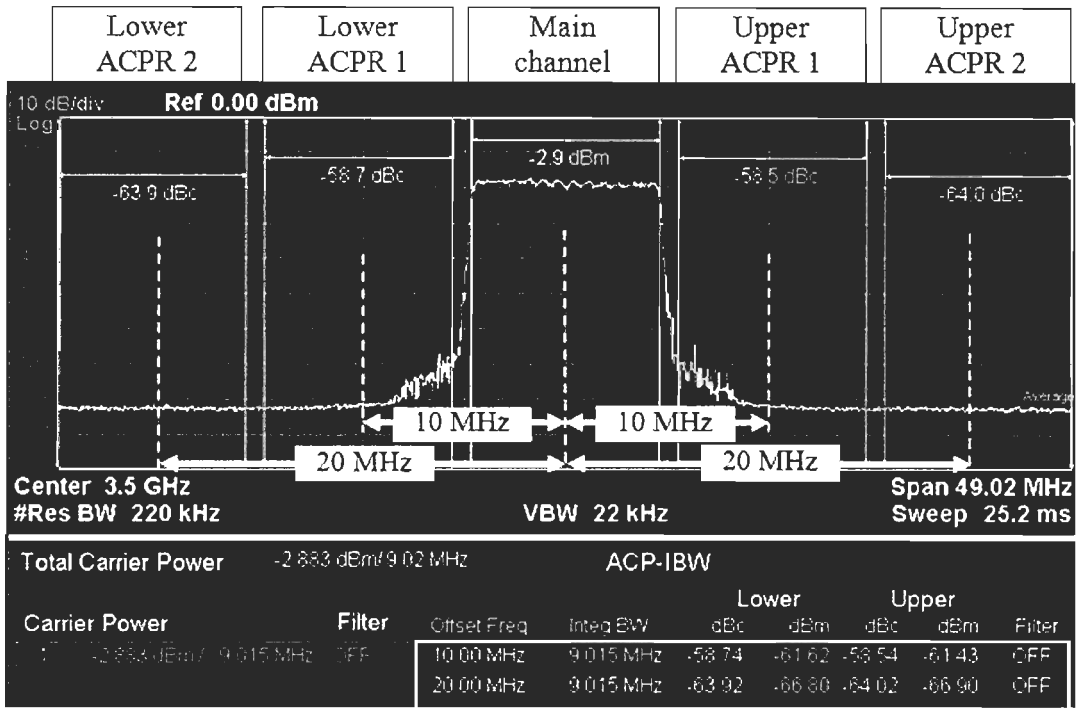


Figure 42 : Setup of the Agilent N9020A MXA signal analyzer for measuring LTE signal

In Agilent N9020A MXA signal analyzer, all the parameters for the LTE measurement are pre-defined according to the LTE standard. With the pre-defined mask for E-TM 1.1 LTE downlink signal with 10 MHz bandwidth, the offset frequency for ACPR 1 and ACPR 2 is 10 MHz and 20 MHz, respectively. During the characterization by the multi-harmonic source & load pull tuner system, the output power, the worst ACPR 1 and ACPR 2 are recorded.

To provide enough input power of the transistor, pre-amplifier is used after the signal generator. The gain, the worst ACPR 1 and ACPR 2 of the pre-amplifier as function of output power of pre-amplifier is shown in Figure 43. The operation range of the pre-amplifier is in the linear region.

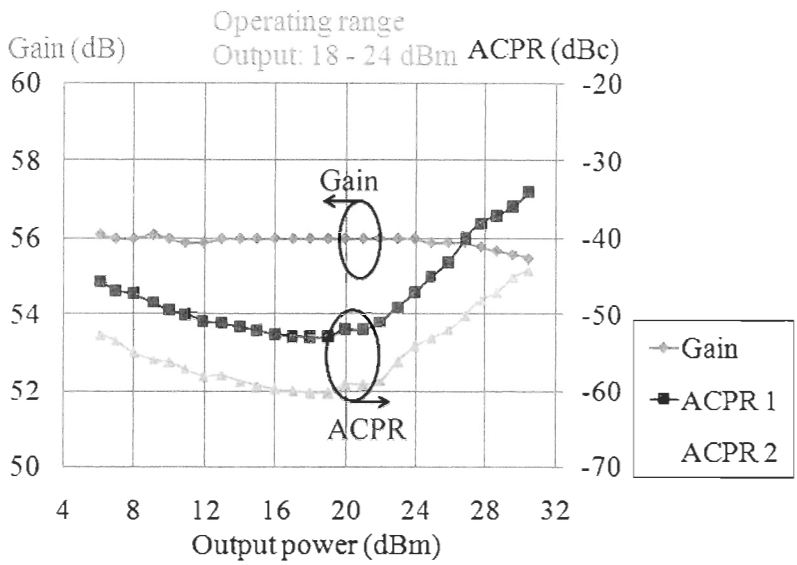


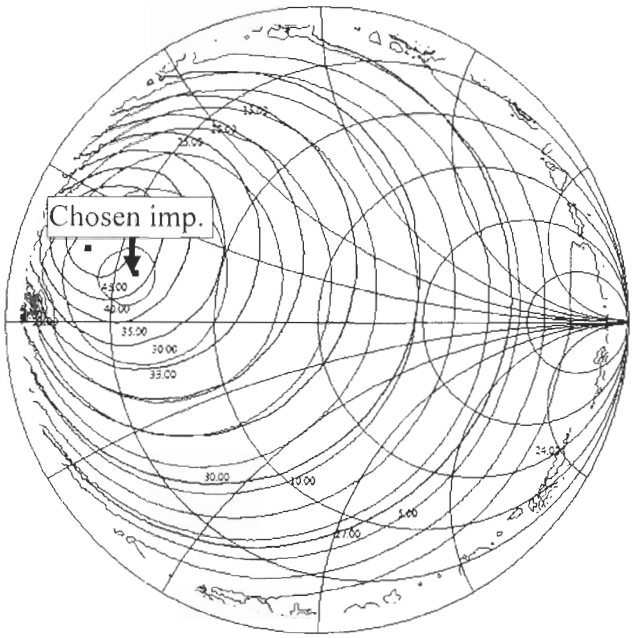
Figure 43 : Gain, worst ACPR 1 and worst ACPR 2 versus output power of pre-amplifier

The characterization of the 10W device CGH40010 transistor by the tuner system is operated at 7 dB back-off power region, so the expected output power is 33 dBm when input power is 18 dBm. Based on the standard of LTE, the worst ACPR 1 and ACPR 2 should be less than -45 dBc at 10 MHz and 20 MHz offset (3GPP org., 2012 e). Previous researches (Draxler *et al.*, 2006; Kimball *et al.*, 2008; cité par Kim *et al.*, 2010a) show that the worst ACPR could be improved by 21 dBc with the DPD linearization technology. Therefore, in the characterization, the worst ACPR 1 and ACPR 2 are expected to be less than -24 dBc. The objective of this characterization with LTE signal by the source & load pull tuner system is obtaining the maximum PAE when the output power is more than 33 dBm and the worst ACPR 1/2 are less than -24 dBc with 18 dBm input power. During the characterization, the transistor is biased at V_{GS}=-2.58 V and V_{DS}=28 V. The strategy of choosing the impedance in each step of characterization is made as follows:

1. For achieving the output power more than 33 dBm and the worst ACPR 1/ACPR 2 less than -24 dBc, we choose the source and load impedances at 3.5 GHz which can provide the maximum output power.

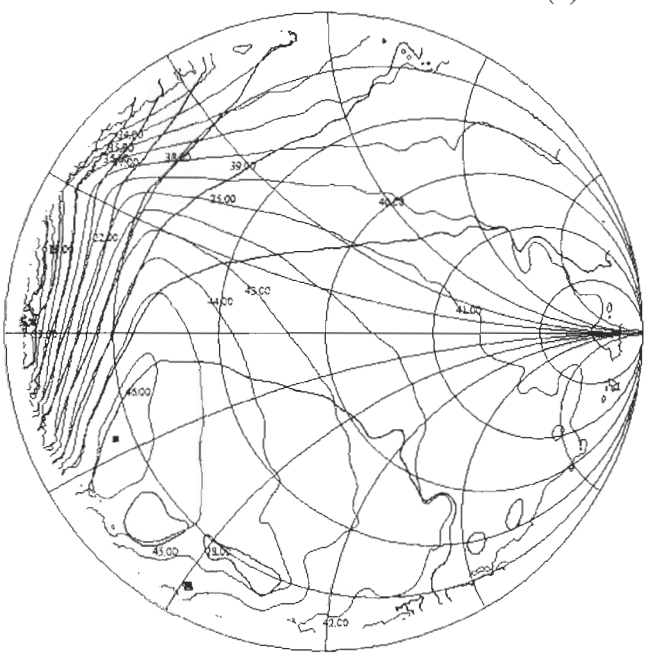
2. For the source and load impedances at the 2nd and 3rd harmonic frequencies, we choose the impedances to increase the PAE, while keep output power more than 33 dBm and keep the worst ACPR 1/ACPR 2 less than -24 dBc.

As a first step of the LTE characterization by the multi-harmonic tuner system, load pull characterization at 3.5 GHz is performed when the source impedance at fundamental frequency is fixed to $0.888\angle -150.1°$. The source & load impedances at the 2nd and 3rd harmonic frequencies are fixed to 50 Ω. The measured PAE, output power, the worst ACPR 1 and ACPR 2 contour is shown in Figure 44. When the load impedance at 3.5 GHz is $0.774\angle 162.4°$, the maximum PAE 50.72% is obtained and the output power is 33.66 dBm, the worst ACPR 1 is -22.06 dBc and the worst ACPR 2 is -39.95 dBc. When the impedance is $0.603\angle 165.5°$, the maximum output power 34.23 dBm is obtained with a PAE of 43.77% and the worst ACPR 1/ACPR 2 of -25.13/-44.36 dBc. The measured minimum ACPR 1 is -28.39 dBc with a PAE of 2.76%, an output power of 24.55 dBm and a worst ACPR 2 of -44.81 dBc, when the impedance is $0.897\angle -118.2°$. The measured minimum ACPR 2 is -46.90 dBc with a PAE of 14.24%, an output power of 30.84 dBm and a worst ACPR 1 of -27.58 dBc, when the impedance is $0.732\angle -152.7°$. In this step, the maximum output power impedance $0.603\angle 165.5°$ is chosen to obtain the output power more than 33 dBm and the worst ACPR 1 or ACPR 2 less than -24 dBc.



	PAE (%)	P_{out} (dBm)
Max	50.72	34.23
1st contour	45.72	33.23
Min	-0.22	-5.56
Step	5.00	1.00

(a)

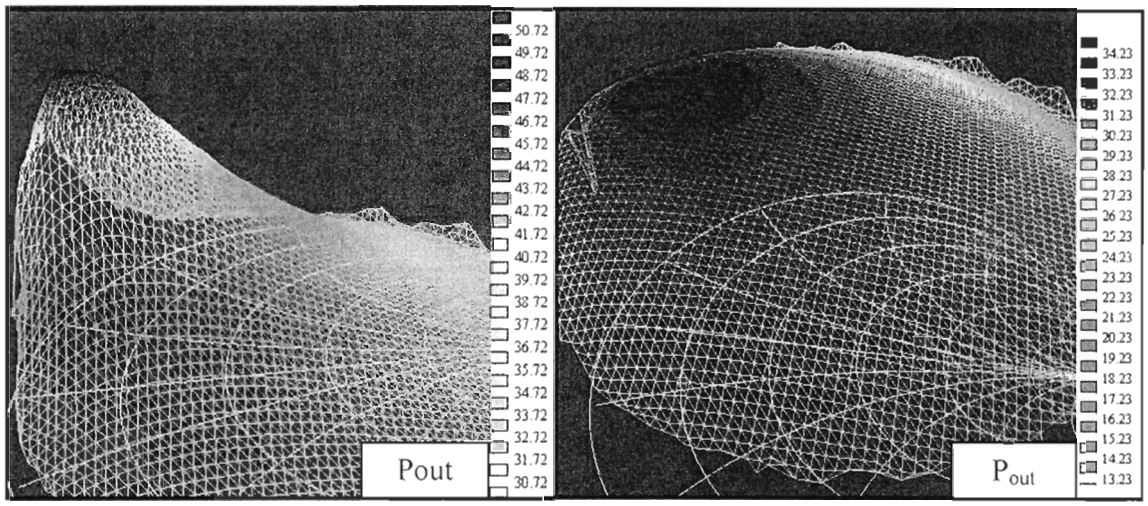


	ACPR 1 (dBc)	ACPR 2 (dBc)
Max	28.39	46.90
1st contour	27.39	45.90
Min	18.02	24.81
Step	1.00	1.00

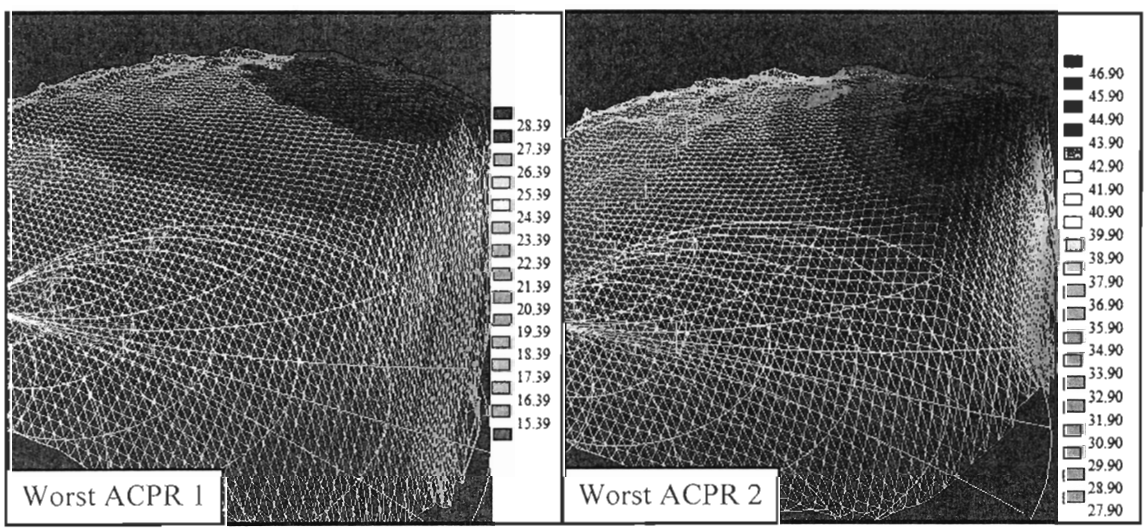
(b)

Figure 44 : Measured PAE & output power contour (a) and the worst ACPR 1 & ACPR 2 contour (b) by the load pull tuner at 3.5 GHz

From the 3D contours in Figure 45, we can see that the PAE, the worst ACPR 1 and worst ACPR 2 are more sensitive to the impedance at fundamental frequency than the output power.



(a) (b)



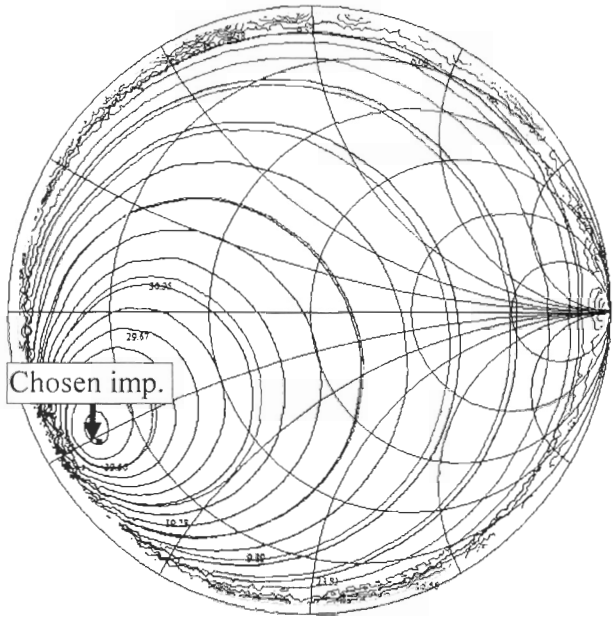
(c) (d)

Figure 45 : Measured PAE (a), output power (b), the worst ACPR 1 (c) and the worst ACPR 2 contour (d) in 3D by the load pull tuner at 3.5 GHz

Then, as a second step, the source pull characterization is done to find the source impedance at the fundamental frequency when the load impedance at the fundamental frequency is fixed to $0.603\angle 165.5°$. The source & load impedances at the 2^{nd} and 3^{rd} harmonic frequencies are fixed to 50 Ω. The source pull characterization result in Figure 46 shows that the maximum PAE and the maximum output power are found at the same source impedance $0.818\angle -148.2°$. At this impedance, the PAE is 44.99% when the output power is 34.45 dBm and the worst ACPR 1/ACPR 2 is -25.34/-43.77 dBc. When the impedance is $0.970\angle -58.6°$, the measured worst ACPR 1 reaches a minimum as -50.17 dBc with a worst ACPR 2 of -44.81 dBc. However, at this impedance point, the PAE is only -0.98% with an output power of 10.72 dBm. When the impedance is $0.859\angle -51.9°$, ACPR 2 reaches a minimum as -60.28 dBc with -44.02 dBc ACPR 1. However, at this impedance, the PAE is only 1.58% with an output power of 21.49 dBm.

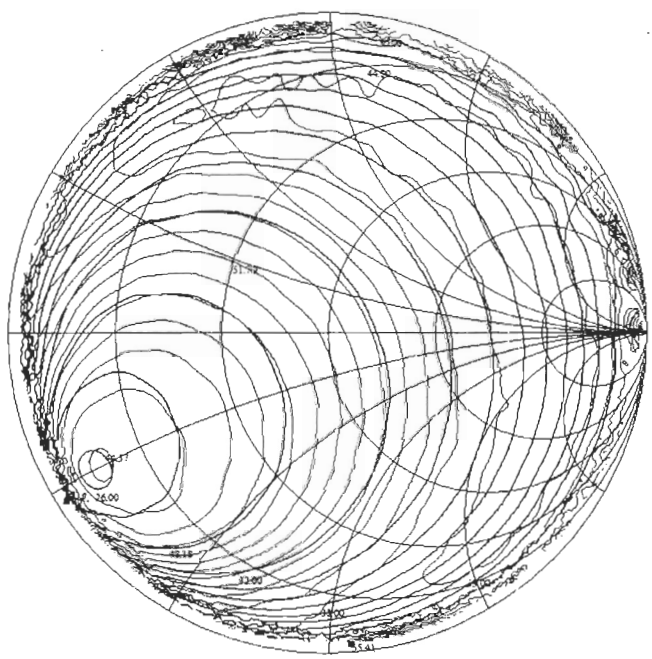
From the 3D contours in Figure 47, we can see that the PAE, the worst ACPR 1 and the worst ACPR 2 are more sensitive to the source impedance at fundamental frequency than the output power. There is a trade-off between the worst ACPR 1/ACPR 2 and the PAE/output power. The impedance with higher PAE/output power deteriorates the ACPR 1 and ACPR 2.

In this step, the maximum PAE/output power impedance $0.818\angle -148.2°$ is chosen for the source impedance at fundamental frequency to obtain the maximum PAE, the output power more than 33 dBm and the worst ACPR 1/ACPR 2 less than -24 dBc.



	PAE (%)	P_{out} (dBm)
Max	44.99	34.45
1st contour	39.99	33.45
Min	-1.16	1.12
Step	5.00	1.00

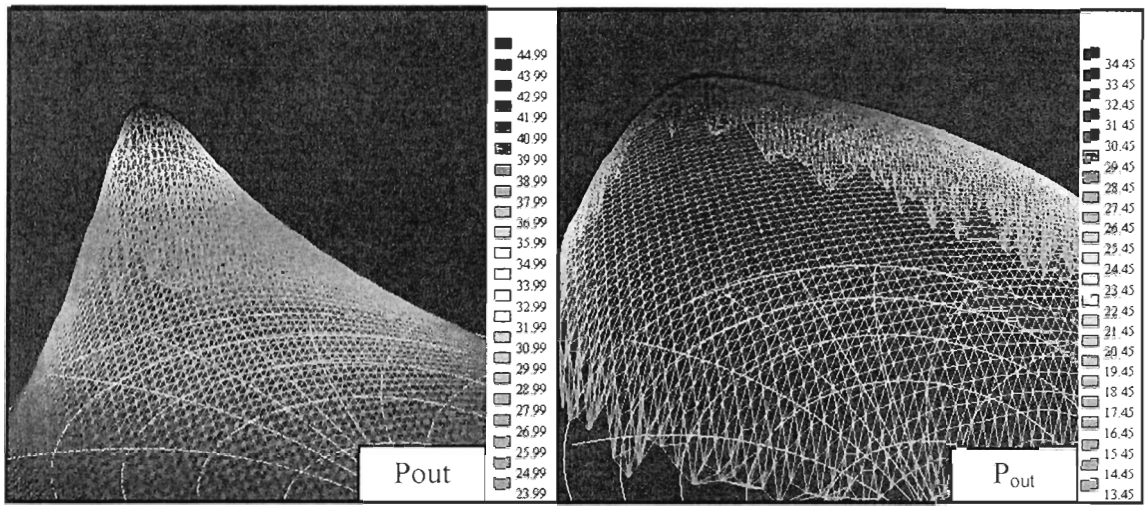
(a)



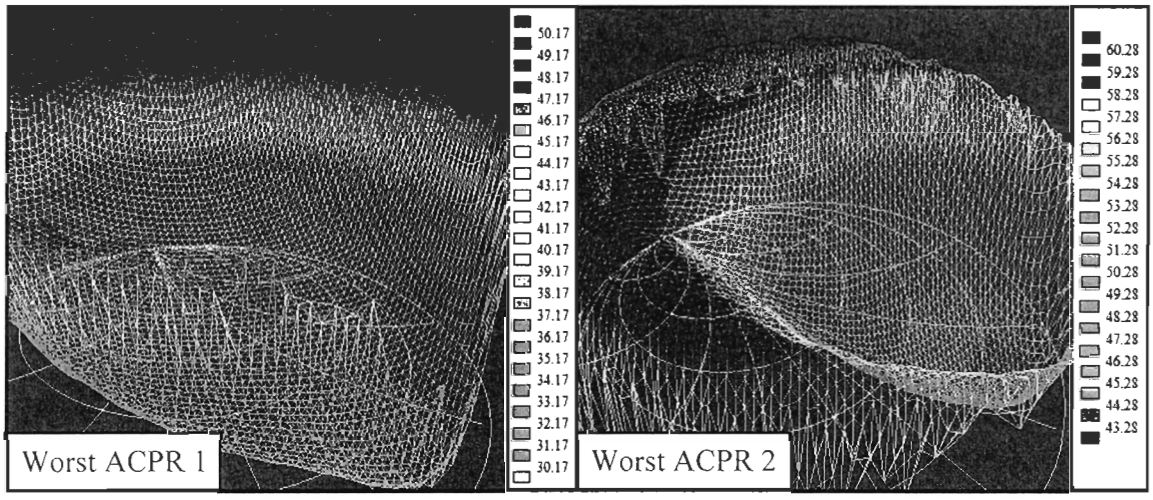
	ACPR 1 (dBc)	ACPR 2 (dBc)
Max	50.17	60.63
1st contour	48.17	58.63
Min	25.17	43.77
Step	2.00	2.00

(b)

Figure 46 : Measured PAE & output power contour (a) and the worst ACPR 1 & ACPR 2 contour (b) by the source pull tuner at 3.5 GHz



(b) (b)



(c) (d)

Figure 47 : Measured PAE (a), output power (b), the worst ACPR 1 (c) and the worst ACPR 2 contour (d) in 3D by the source pull tuner at 3.5 GHz

The next step is sweeping the load impedance at the 2^{nd} and 3^{rd} harmonic frequencies by the source & load pull tuner system. First, the load impedance at the 2^{nd} harmonic frequency is tuned when the source and load impedances at fundamental frequency are fixed to the values which are found in the previous steps (Source impedance at fundamental

frequency: 0.818∠-148.2° and load impedance at fundamental frequency: 0.603∠165.5°). The load impedance at the 3rd harmonic frequency and the source impedances at the 2nd and 3rd harmonic frequencies are fixed to 50 Ω. Figure 48 shows the measured PAE by the load pull tuner at 7 GHz. PAE is increased to 47.50% with 33.87 dBm output power and -25.34/-43.51 dBc ACPR 1/ACPR 2 by tuning the load impedance at the 2nd harmonic frequency to 0.923∠-166.6°. In this step, the PAE is increased by 2.50% by tuning the load impedance at the 2nd harmonic frequency.

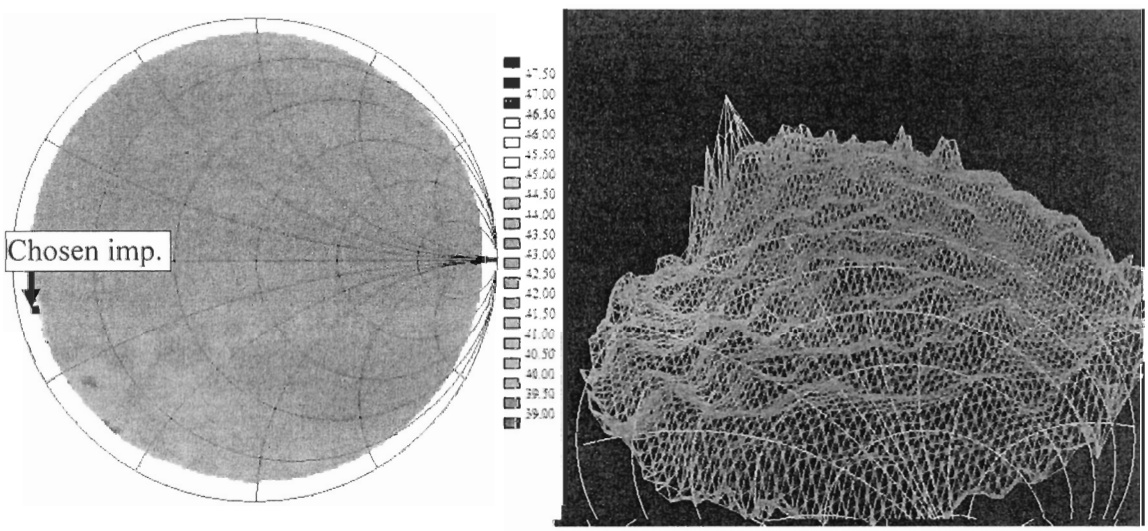


Figure 48 : Measured PAE contour by the load pull tuner at 7 GHz

The measured PAE, output power, the worst ACPR 1 and the worst ACPR 2 versus the phase of the load impedance at 7 GHz when the Γ of load impedance at 7 GHz is maintained as close as possible to 1 are shown in Figure 49. We can see that the PAE is more sensitive to the phase of the load impedance at 7 GHz compared to the output power, the worst ACPR 1 and the worst ACPR 2. If the phase of the load impedance at the 2nd harmonic frequency is -141.1°, the PAE is reduced from 47.50% to 38.45% with 33.71 dBm output power and -26.26/-44.13 dBc ACPR 1/ACPR 2.

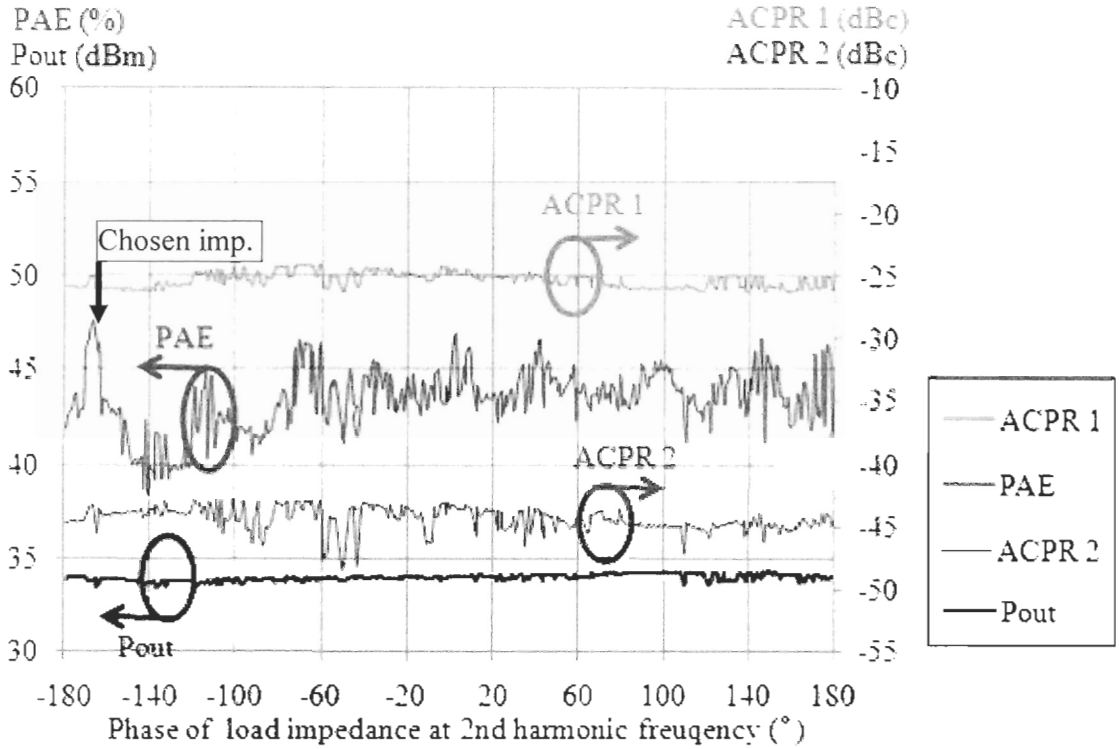


Figure 49 : Measured PAE, output power, the worst ACPR 1 and the worst ACPR 2 versus the phase of the load impedance at 7 GHz by the tuner system with the LTE signal

As a fourth step, the load impedance at 10.5 GHz is tuned by the load pull tuner. The source impedance at 3.5 GHz is 0.818∠-148.2° and the load impedance at 3.5 GHz is 0.603∠165.5°. The load impedance at 7 GHz is fixed to 0.923∠-166.6° and the source impedances at the 2nd and 3rd harmonic frequencies are fixed to 50 Ω. The measured PAE in Figure 50 shows when the impedance at 10.5 GHz is 0.920∠86.1°, the PAE reaches the maximum as a 47.98% with 33.82 dBm output power and -25.16/-43.45 dBc ACPR 1/ACPR 2. By tuning the load impedance at 10.5 GHz, the PAE is increased by 0.48%.

The measured PAE, output power, ACPR 1 and ACPR 2 versus the phase of the load impedance at 10.5 GHz when the Γ of load impedance at 10.5 GHz is maintained as close as possible to 1 are shown in Figure 51. If the phase of the load impedance at 10.5 GHz is 164.6°, the PAE is reduced from 47.98% to 39.87% with 33.92 dBm output power,

-26.41/-45.54 dBc ACPR 1/ACPR 2. Figure 51 shows that the PAE is more sensitive to the phase of the load impedance at 10.5 GHz compared to the output power, ACPR 1/ACPR 2.

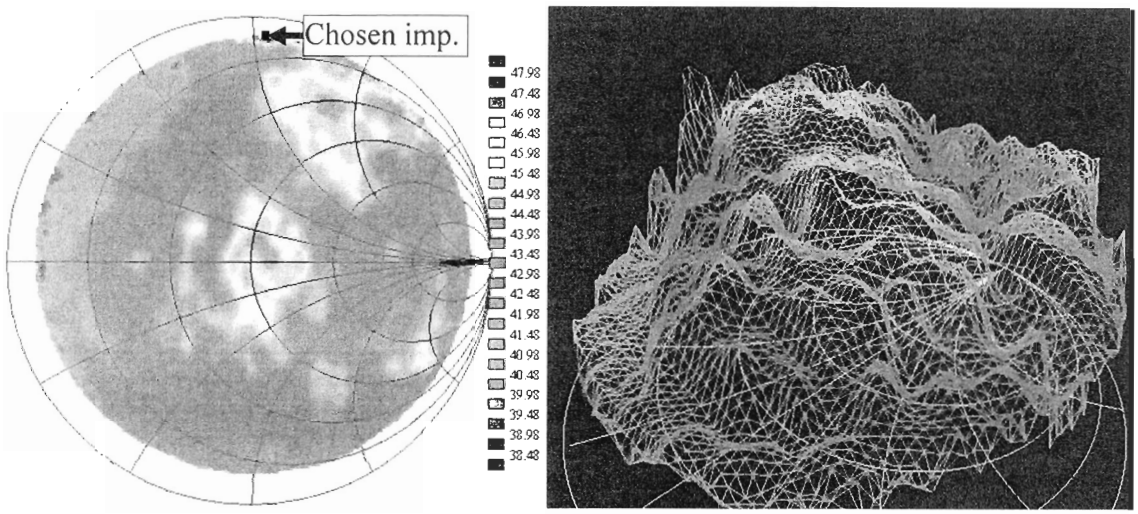


Figure 50 : Measured PAE contour by the load pull tuner at 10.5 GHz

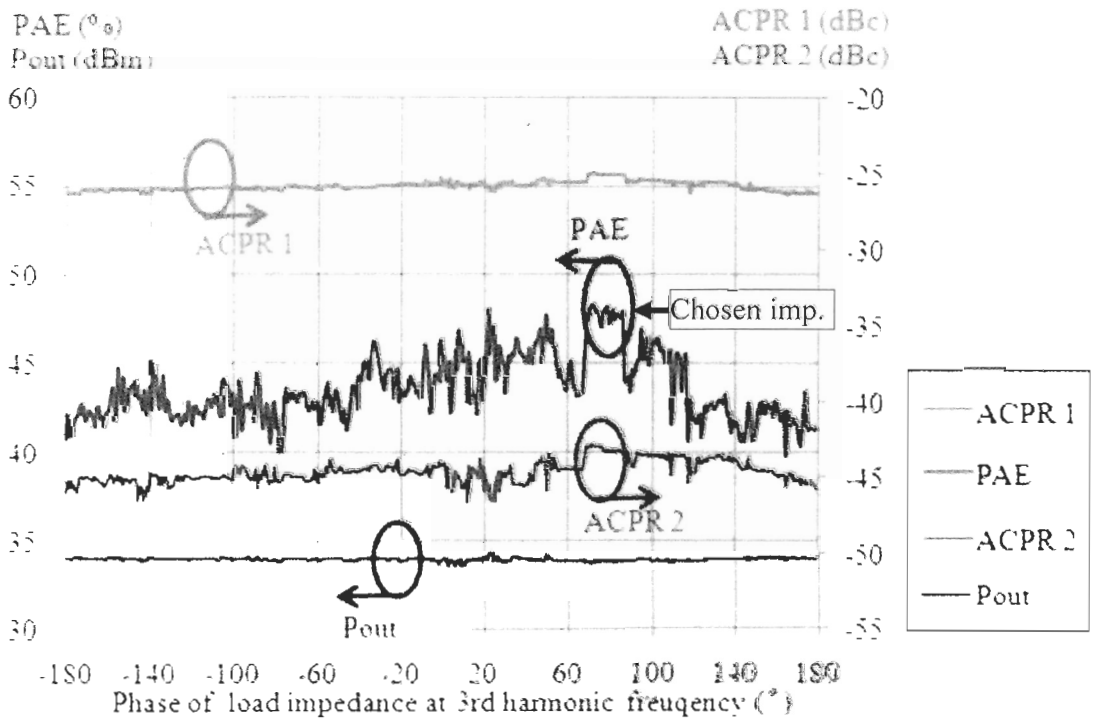


Figure 51 : Measured PAE, output power, the worst ACPR 1 and the worst ACPR 2 versus the phase of the load impedance at 10.5 GHz by the tuner system with the LTE signal

After tuning the load impedance at the 3rd harmonic frequency, the source impedance at the 2nd harmonic frequency is tuned. The source and load impedance at the fundamental frequency are fixed to 0.818∠-148.2° and 0.603∠165.5°, respectively. The load impedances at the 2nd and 3rd harmonic frequencies are fixed to 0.923∠-166.6° and 0.920∠86.1°, respectively. The source impedance at the 3rd harmonic frequency is fixed to 50 Ω. The measured PAE in Figure 52 shows that when the source impedance at the 2nd harmonic frequency is 0.929∠147.5°, the PAE reaches the maximum as a 50.83% with 34.31 dBm output power and -24.31/-42.58 dBc ACPR 1/ACPR 2. By considering the source 2nd harmonic, the PAE is increased by 2.85%.

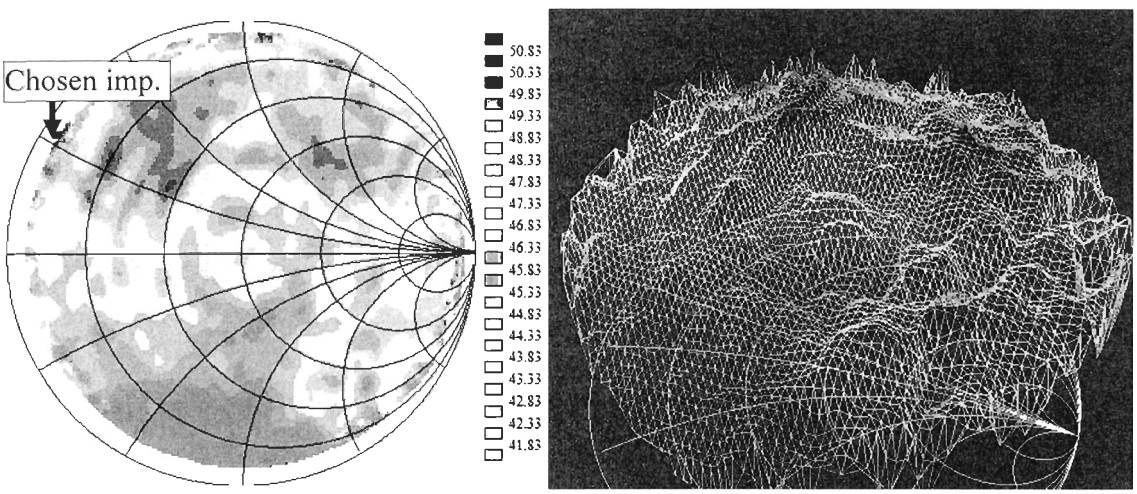


Figure 52 : Measured PAE contour by the source pull tuner at 7 GHz

The measured PAE, output power, ACPR 1 and ACPR 2 versus the phase of the source impedance at 7 GHz when the Γ of source impedance at 7 GHz is maintained as close as possible to 1 are shown in Figure 53. We can see that the PAE is more sensitive to the phase of the source impedance at 7 GHz compared output power, ACPR 1 and ACPR 2. If the phase of the source impedance at the 2nd harmonic frequency is -86.3°, the PAE is reduced from 50.83% to 35.5% with 32.47 dBm output power, -26.31/-45.19 dBc ACPR 1/ACPR 2.

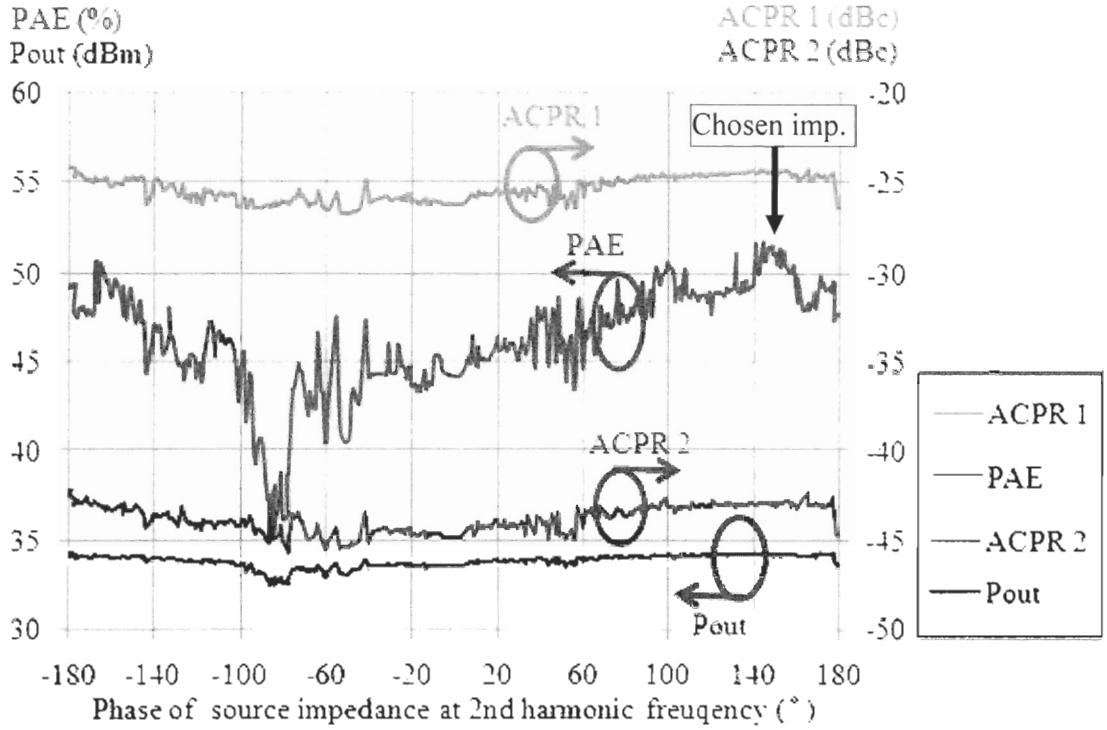


Figure 53 : Measured PAE, output power, the worst ACPR 1 and the worst ACPR 2 versus the phase of the source impedance at 7 GHz by the tuner system with the LTE signal

At last, the source impedance at the 3rd harmonic frequency is tuned. By tuning the source impedance at the 3rd harmonic frequency, the characterization result in Figure 54 shows when the source impedance at the 3rd harmonic frequency is $0.919\angle 94.8°$, the maximum PAE 51.48% can be obtained with 34.24 dBm output power and -24.23/-42.40 dBc worst ACPR 1/ACPR 2. In the last step, the PAE is increased the by 0.65% by tuning the source impedance at the 3rd harmonic frequency.

The measured PAE, output power, ACPR 1 and ACPR 2 versus the phase of the source impedance at 10.5 GHz when the Γ of source impedance at 10.5 GHz is maintained as close as possible to 1 are shown in Figure 55. It is worth to notice that the PAE, output power, ACPR 1 and ACPR 2 are all sensitive to the phase of the source impedance at 10.5 GHz. If the phase of the source impedance at the 3rd harmonic frequency is -85.1°, the PAE is reduced from 51.48% to 16.03% with 29.18 dBm output power and -28.72/-50.72 dBc ACPR 1/ACPR 2.

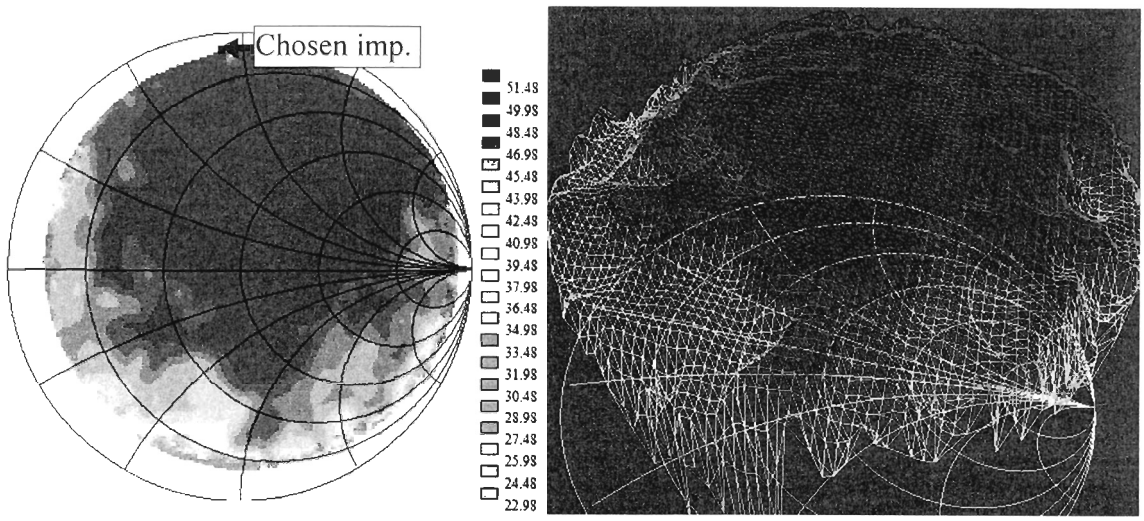


Figure 54 : Measured PAE contour by the source pull tuner at 10.5 GHz

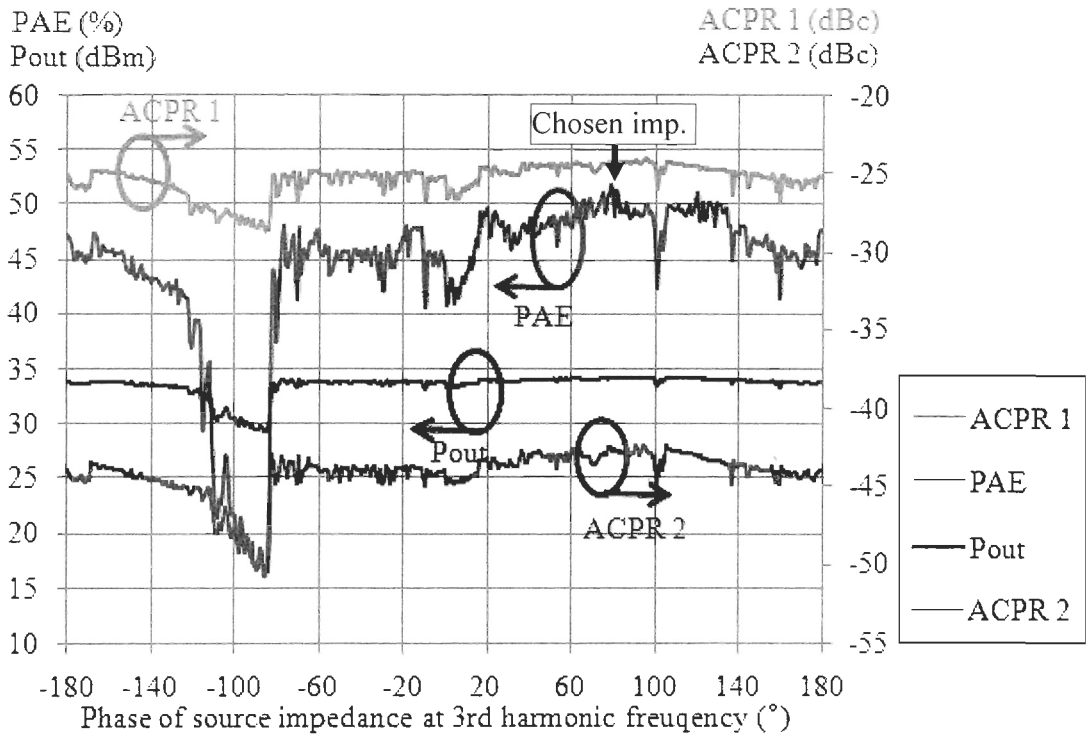


Figure 55 : Measured PAE, output power, the worst ACPR 1 and the worst ACPR 2 versus the phase of the source impedance at 10.5 GHz by the tuner system with the LTE signal

With this proposed characterization procedure, the chosen source and load impedances at the fundamental frequency, the 2nd harmonic and 3rd harmonic frequencies could offer 51.48% PAE when the output power is 34.24 dBm with the worst ACPR 1/ACPR 2 less than -24 dBc.

Table 10 summarizes the procedure of LTE characterization by the source & load pull tuner system. From Table 10, we can see that the PAE is increased by 2.50% by tuning the load impedance at the 2nd harmonic frequency. By tuning the load impedance at the 3rd harmonic frequency, the PAE is increased by 0.48%. By tuning the source impedance at the 2nd harmonic frequency, the PAE is increased by 2.85%. 3rd harmonic in the source increases the PAE by 0.65%. During the characterization, the worst ACPR 1 and the worst ACPR 2 are always less than -24 dBc.

Table 10 : LTE characterization result obtained by the source & load pull tuner system

	Frequency (GHz)	Source impedance	Load impedance	PAE (%)	P_{out} (dBm)	ACPR 1 ACPR 2 (dBc)
Step 1 Load pull @ 3.5 GHz	3.5	0.888∠-150.1°	0.603∠165.4°	43.77	34.23	-25.13 -44.36
	7	0∠0°	0∠0°			
	10.5	0∠0°	0∠0°			
Step 2 Source pull @ 3.5 GHz	3.5	0.818∠-148.2°	0.603∠165.4°	45.00	34.45	-25.34 -43.77
	7	0∠0°	0∠0°			
	10.5	0∠0°	0∠0°			
Step 3 Load pull @ 7 GHz	3.5	0.818∠-148.2°	0.603∠165.4°	47.50	33.87	-25.34 -43.51
	7	0∠0°	0.923∠-166.6°			
	10.5	0∠0°	0∠0°			
Step 4 Load pull @ 10.5 GHz	3.5	0.818∠-148.2°	0.603∠165.4°	47.98	33.82	-25.16 -43.45
	7	0∠0°	0.923∠-166.6°			
	10.5	0∠0°	0.929∠86.1°			
Step 5 Source pull @ 7 GHz	3.5	0.818∠-148.2°	0.603∠165.4°	50.83	34.31	-24.31 -42.58
	7	0.929∠147.5°	0.923∠-166.6°			
	10.5	0∠0°	0.929∠86.1°			
Step 6 Source pull @ 10.5 GHz	3.5	0.818∠-148.2°	0.603∠165.4°	51.48	34.24	-24.23 -42.40
	7	0.929∠147.5°	0.923∠-166.6°			
	10.5	0.919∠94.8°	0.929∠86.1°			

The characterization results obtained by the multi-harmonic source & load pull tuner with the LTE signal and 1-tone signal is compared in the following figure and table.

Table 11 : Comparison of the characterization results obtained by the multi-harmonic source & load pull tuner with the LTE signal and 1-tone signal, where f_0 is 3.5 GHz

	1-tone characterization results obtained by the source & load pull tuner		**LTE characterization results obtained by the source & load pull tuner**	
Step 1 Load pull @ f_0	Load imp. @ f_0: $0.603\angle 165.4°$	PAE: 62.41% P_{out}: 40.47 dBm	Load imp. @ f_0: $0.603\angle 165.4°$	PAE: 43.77% P_{out}: 34.23 dBm ACPR 1: -25.13 dBc ACPR 2: -44.36 dBc
Step 2 Source pull @ f_0	Source imp. @ f_0: $0.892\angle -151.7°$	PAE: 64.33% P_{out}: 40.07 dBm	Source imp. @ f_0: $0.818\angle -148.2°$	PAE: 45.00% P_{out}: 40.07 dBm ACPR 1: -25.34 dBc ACPR 2: -43.77 dBc
Step 3 Load pull @ $2f_0$	Load imp. @ $2f_0$: $0.938\angle 146.1°$	PAE: 68.48% P_{out}: 40.06 dBm	Load imp. @ $2f_0$: $0.923\angle -166.6°$	PAE: 47.50% P_{out}: 33.87 dBm ACPR 1: -25.34 dBc ACPR 2: -43.51 dBc
Step 4 Load pull @ $3f_0$	Load imp. @ $3f_0$: $0.918\angle 42.6°$	PAE: 69.42% P_{out}: 40.01 dBm	Load imp. @ $3f_0$: $0.929\angle 86.1°$	PAE: 47.98% P_{out}: 33.82 dBm ACPR 1: -25.16 dBc ACPR 2: -43.45 dBc
Step 5 Source pull @ $2f_0$	Source imp. @ $2f_0$: $0.900\angle -38.5°$	PAE: 73.08% P_{out}: 39.83 dBm	Source imp. @ $2f_0$: $0.929\angle 147.5°$	PAE: 50.83% P_{out}: 34.31 dBm ACPR 1: -24.31 dBc ACPR 2: -42.58 dBc
Step 6 Source pull @ $3f_0$	Source imp. @ $3f_0$: $0.880\angle -68.6°$	PAE: 74.21% P_{out}: 39.92 dBm	Source imp. @ $3f_0$: $0.919\angle 94.8°$	PAE: 51.48% P_{out}: 34.24 dBm ACPR 1: -24.23 dBc ACPR 2: -42.40 dBc

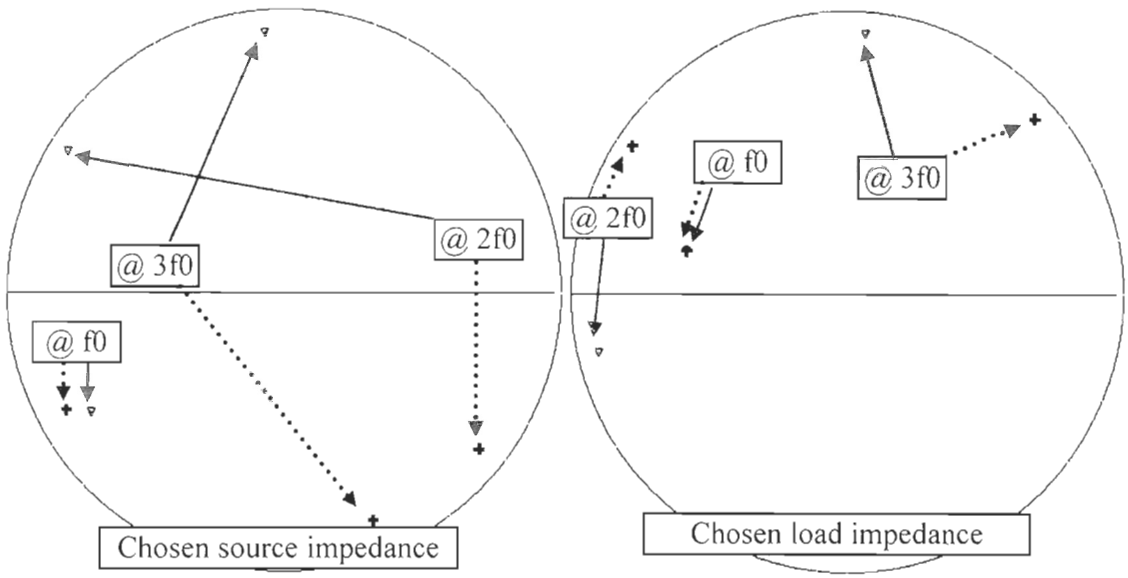


Figure 56 : Source and load impedance at the fundamental, 2nd and 3rd harmonic frequencies found by the source & load pull tuner system with the LTE signal and 1-tone signal, where f_0 is 3.5 GHz

From the comparison, we can see that, the chosen source and load impedances at 3.5 GHz are similar. The load impedances at 3.5 GHz found in the characterizations with the LTE and 1-tone signal are same. For the source impedances at 3.5 GHz found in the characterizations with the LTE and 1-tone signal, there are 0.074 difference in magnitude and 3.5° difference in phase. The chosen impedances at harmonic frequencies for the LTE signal and 1-tone signal are different. For the load impedances at the 2nd harmonic, there is 47.3° difference in phase. For the load impedances at the 3rd harmonic, there is 43.5° difference in phase. For the source impedances at the 2nd harmonic, there is 174.0° difference in phase. For the source impedances at the 3rd harmonic, there is 163.4° difference in phase. Because the characterization with LTE signal is operated with 7 dB back-off, the output power and PAE in the final step of the characterization with LTE signal are 5.68 dBm and 22.73% lower than the output power and PAE obtained in the characterization with 1-tone signal by the tuner system, respectively. In this case, with

different types of signal, the chosen impedances at fundamental frequency are similar, but the chosen impedances at harmonic frequencies are different.

2.6 CONCLUSION

In this work, to design an inverse class F PA, the Cree's CGH40010 transistor is characterized and analyzed first by using a large signal model in the source & load pull simulation in ADS 2011.10 with 1-tone signal at 3.5 GHz. Then, the multi-harmonic source & load pull tuner system from Focus microwaves Inc. is used to characterize and analyze the real transistor device with a 1-tone and a LTE signal. All the characterization results indicate that not only the load 2^{nd} and 3^{rd} harmonic are important to achieve the high PAE and output power for an inverse class F PA, but also the source 2^{nd} and 3^{rd} harmonic. And the Γ of the impedances at the harmonic frequencies should be as near 1 as possible, so that the high PAE could be achieved. However, by comparing the characterization results obtained by different methods, we found that the simulation with the transistor's large signal model does not offer the same results as the multi-harmonic tuner system, such as PAE, output power and source/load impedances at the 2^{nd} and 3^{rd} harmonic frequencies. In order to evaluate these characterization results, PAs should be designed, fabricated, measured. We will compare the measured results of the PAs fabricated based on the characterization results to determine the most precise method of characterization. This work is shown in chapter 5.

In this chapter, our contribution is that we proposed a methodology to characterize and analyze the transistor by the multi-harmonic tuner system with considering the 2^{nd} and 3^{rd} harmonic on both input and output side of the transistor simultaneously when the transistor is excited with 1-tone and LTE signal. Based on the references, the most of the authors only considered the load impedances at the 2^{nd} and 3^{rd} harmonic frequencies by ignoring the source impedance at the 2^{nd} and 3^{rd} harmonic frequencies. It is the first time that both the source and load 2^{nd} and 3^{rd} harmonic are considered in the characterization by

the multi-harmonic source & load pull tuner system with 1-tone and LTE signal. And by using the multi-harmonic tuner system, we proved the importance of the source impedance at the 2nd and 3rd harmonic frequencies for an inverse class F PA with 1-tone signal and LTE signal. If the source impedances at the 2nd and 3rd harmonic frequencies are not well tuned, the PAE of the inverse class F PA could be reduce. Therefore, the source impedances at the 2nd and 3rd harmonic frequencies should be considered to maximize the PAE when the inverse class F PA is designed.

The publication related to the work in this chapter is referenced as below:

GAO, Shengjie and Chan-Wang PARK. 2012. « Large signal characterization of GaN HEMT transistor by multi-harmonic source & load pull tuner system ». In *IEEE ARFTG Microwave Measurement Symposium.* (San Diego, CA, 27-30 November 2012).

CHAPITRE 3
CONTOUR METHOD TO SHIFT THE CALIBRATED REGION OF SOURCE/LOAD PULL TUNERS IN POWER AMPLIFIER CHARACTERIZATION

3.1 RÉSUMÉ

Dans ce chapitre, une méthode de déplacement de la région calibrée du *tuner source/load pull* passif par le choix des accessoires est introduit. Cette méthode permet d'augmenter le coefficient de réfection (Γ) du *tuner source/load pull* passif à plan de référence DUT dans une région désirée de l'abaque de Smith. La région calibrée du *tuner source/load pull* peut être déplacée intentionnellement à la région souhaitée en choisissant les accessoires du système *source/load pull tuner*, comme le té de polarisation, le coupleur directionnel, l'isolateur et l'atténuateur. L'effet du déplacement de la région calibrée du *tuner source/load pull* par ces accessoires est analysé. Sur la base de cette analyse, les accessoires sont sélectionnés pour déplacer intentionnellement la région calibrée du *tuner source/load pull* à la région désirée et augmenter la Γ maximale.

3.2 ABSTRACT

In this chapter, a method is introduced to shift the calibrated region of the passive source/load pull tuners by choosing accessories. This method aims to increase the reflection coefficient (Γ) of the passive source/load pull tuner system at the device under test (DUT) reference plane in a target region of Smith chart. The calibrated region of the tuner can be

shifted intentionally to the desired region by choosing the accessories, such as the bias tee, the directional coupler, the isolator and the attenuator, in the tuner system while considering the phase and magnitude of their S-parameters. The effect of the shifting of the calibrated region is analyzed. Based on this analysis, the accessories are chosen to shift the calibrated region of the passive tuner system intentionally to the target region and increase the maximum Γ.

3.3 INTRODUCTION

For the purpose of designing a PA in nonlinear region, source/load pull technique as a large signal characterization method is used to characterize a microwave power transistor (Hoversten *et al.*, 2010). There are two types of source/load pull techniques: active and passive source/load pull.

The active load pull systems can tune the load impedance at the DUT reference plane by use virtual load: part of the outgoing signal is modified in amplitude and phase by an amplifier/phase-shifter network and re-injected into the output port of the DUT. The advantage of the active source/load pull tuner is that it could realize the impedance with high Γ (more than 1), because of the amplification involved. However, oscillation may occur, since the DUT is part of the active loop (Focus microwaves Inc., 2012b).

The passive load pull tuner, as shown in Figure 3, can tune the load impedance at the DUT reference plane by changing the position of the probes in the tuner. The advantage of the passive tuner is that it has higher power handling capability compared with the active tuner (Ghannouchi *et al.*, 2010; Hashmi *et al.*, 2011), but the maximum Γ of the passive tuner system is lower than the active tuner (typically in the range 0.800 and 0.920) due to the limit of the probe in the passive tuner and the losses incurred in the passive tuner (Agilent technologies Inc., 2011). Based on the characterization results of CGH40010 transistor in chapter 2, we can see that high Γ is important when the transistor is

characterized for inverse class F operation, because higher Γ could increase the output power and PAE of PA.

(Hashmi *et al.*, 2011) introduced the pre-matching tuner to increase the maximum Γ of the passive source/load pull tuner system. Pre-matching tuners employ two independent RF probes to increase the Γ (Focus microwaves Inc., 2012a). To achieve a high Γ, one of the probes moves the matched condition to the desired region of the Smith chart, while the other probe forms the loci of the reflection coefficient around this new matched position as shown in Figure 57 (Hashmi *et al.*, 2011). Based on (Focus microwaves Inc., 1999 et Maury microwave Inc., 2000; cités par Hashmi *et al.*, 2011), the maximum Γ could be increased from 0.750 to 0.920 by using the pre-matching tuner.

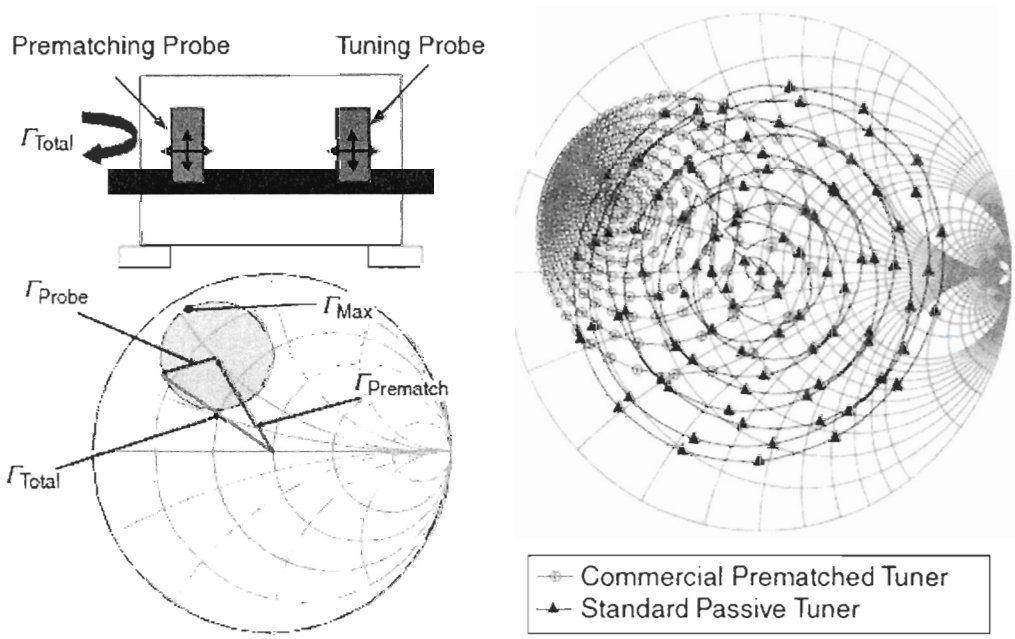


Figure 57 : Pre-matched impedance tuning concept (Hashmi *et al.*, 2011)

However, in our case, for the Focus microwaves' multi-harmonic source & load pull tuner, there are only 3 probes in the tuner to control 3 frequencies. If we use 2 probes to increase Γ at one frequency, we cannot control 3 frequencies at same time. Thus, we cannot

employ the pre-matching network technology if we want to control 3 frequencies at the same time by using the multi-harmonic source & load pull tuner.

Ghannouchi *et al.* proposed to add an extra passive loop structure in the source/load pull tuner system to increase Γ as shown in Figure 58 (Ghannouchi *et al.*, 2010). With this method, the maximum Γ of source pull tuner could be increased from 0.850 to 0.950. The maximum Γ of load pull tuner could be increased from 0.750 to 0.970.

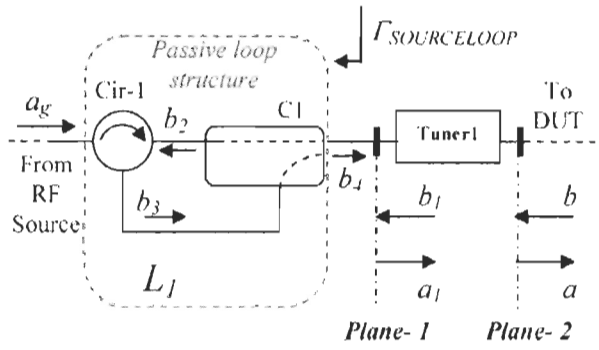


Figure 58 : The improved passive source pull tuner topology for achieving high Γ (Ghannouchi *et al.*, 2010)

In our case, we do not want to add extra component in the source & load pull tuner system. Therefore, how to increase the maximum Γ of the passive multi-harmonic tuner system without adding extra components in the system is the question.

In this work, we propose a novel method to increase the maximum Γ by choosing the accessories which are needed in the source/load pull tuner system, such as the bias tee, the directional coupler and the isolator. The proposed method can be described as follows: First, analyze the effect of the accessories in the tuner system on the maximum Γ of the passive tuner system. Then, based on the analysis, choose the accessories to increase the maximum Γ of the passive tuner system. By this method, the maximum Γ of the passive tuner system can be increased without adding any extra accessories in the passive tuner system.

3.4 ANALYSIS OF EFFECT OF ACCESSORY ON MAXIMUM Γ OF THE PASSIVE SOURCE/LOAD PULL TUNER SYSTEM

Before using the passive source/load pull tuners, they should be calibrated by VNA. During the calibration of tuner, the S-parameters as a function of tuner probe positions are recorded. Figure 59 shows the calibration setup for the source pull tuner. The computer in Figure 59 controls the source pull tuner probe positions. For each tuner probe position, VNA measures the S-parameters S'' of the source pull tuner. Then the measured S-parameters S'' are recorded with their corresponding tuner probe positions by the computer. The black points in Figure 60 present the measured S''_{22} of source pull tuner. And each measured S''_{22} points correspond to a unique tuner probe position. We define the measured S''_{22} points in Figure 60 as the calibrated impedance points. The region covered by the calibrated points is defined as the calibrated region. In our case, the measured maximum reflection coefficient Γ of calibrated S''_{22} impedance points is 0.930.

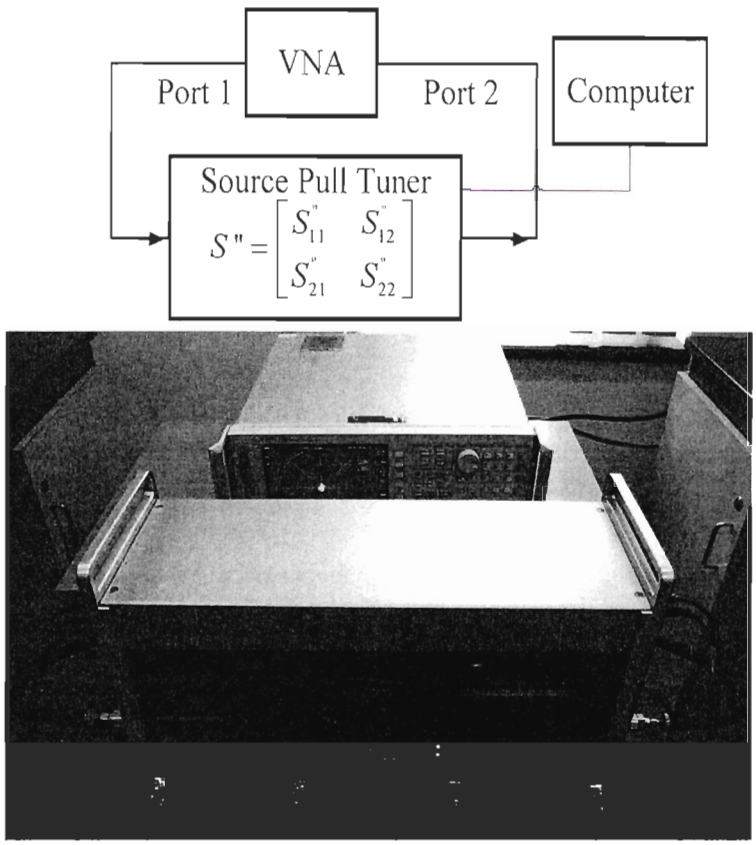


Figure 59 : Setup for calibrating the source pull tuner

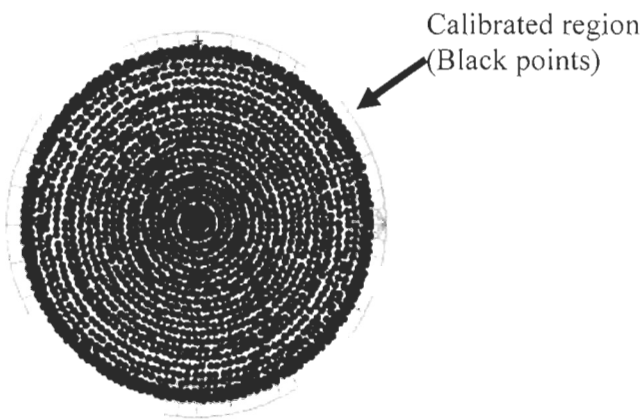


Figure 60 : Calibrated region of the source pull tuner

Then, in order to see the effect of the accessory on the calibrated region, an accessory is added in the source pull system. The accessory, such as the bias tee, the isolator or the directional coupler, is usually added on the left side of the source pull tuner. Figure 61 shows the setup for the source pull tuner with the accessory. In Figure 61, the total block consists of a source pull tuner with accessory. Γ is the reflection coefficient of S_{22} at the DUT reference plane. Γ' is the reflection coefficient of S'_{22} of the accessory. Γ'' is the reflection coefficient of S''_{22} of the source pull tuner.

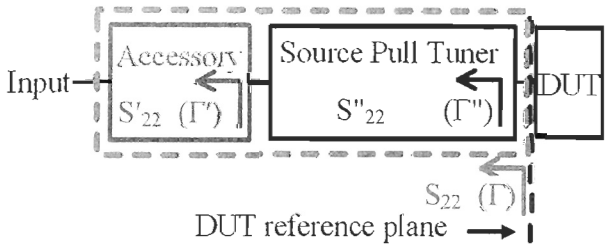


Figure 61 : Setup for the source pull tuner with the accessory

S_{22} of total block shown in Figure 61 at the DUT reference plane can be expressed as (Dobrowolski, 2010),

$$S_{22} = S''_{22} + \frac{S''_{21}S''_{12}S'_{22}}{1 - S''_{11}S'_{22}} \tag{7}$$

where S''_{11}, S''_{22}, S''_{12} and S''_{21} are the S-parameter of the source pull tuner alone and S'_{22} is for the accessory. According to (7), for one fixed calibrated impedance point (S") of the source pull tuner in Figure 60, only S'_{22} of the accessory could affect the S_{22} at the DUT reference plane for the source pull tuner.

To show the effect of S'_{22} of the accessory on the calibrated impedance points of the tuner, as a first step, we choose one calibrated impedance point S" of the source pull tuner (filled circle in Figure 62) as shown in (8).

$$S'' = \begin{pmatrix} S''_{11} & S''_{12} \\ S''_{21} & S''_{22} \end{pmatrix} = \begin{pmatrix} 0.926\angle 90.5° & 0.304\angle 3.1° \\ 0.305\angle 3.1° & 0.917\angle 90.9° \end{pmatrix} \quad (8)$$

For this calibrated impedance point, $S''_{22}=0.917\angle 90.9°$. Then, we add an accessory with $S'_{22}=0.200\angle 0.0°$ on the left side of the source pull tuner. Based on (7), S_{22} could be calculated as shown in (9).

$$\begin{aligned} S_{22} &= S''_{22} + \frac{S''_{21}S''_{12}S'_{22}}{1-S''_{11}S'_{22}} \\ &= 0.917\angle 90.9° + \frac{(0.305\angle 3.1°)(0.304\angle 3.1°)(0.2\angle 0°)}{1-(0.926\angle 90.5°)(0.2\angle 0°)} \\ &= 0.917\angle 90.9° + \frac{0.019\angle 6.2°}{1.019\angle -10.5°} \\ &= 0.922\angle 89.8° \end{aligned} \quad (9)$$

To analyze the effect of the phase change of S'_{22} on S_{22}, S_{22} is simulated with $S'_{22}=0.200\angle 90.0°$, $0.200\angle 180.0°$ and $0.200\angle -90.0°$. The simulated S_{22} are plotted on the Smith chart in Figure 62. As shown in Figure 62, after adding the accessory with $S'_{22}=0.200\angle 90.0°$, Γ is increased from 0.917 to 0.932 at the DUT reference plane. However, when the accessory with $S'_{22}=0.200\angle -90.0°$ is added, Γ is reduced from 0.917 to 0.894. For the accessory with $S'_{22}=0.200\angle 0.0°$ and $0.200\angle 180.0°$, Γ is changed from 0.917 to 0.922 and 0.918, respectively.

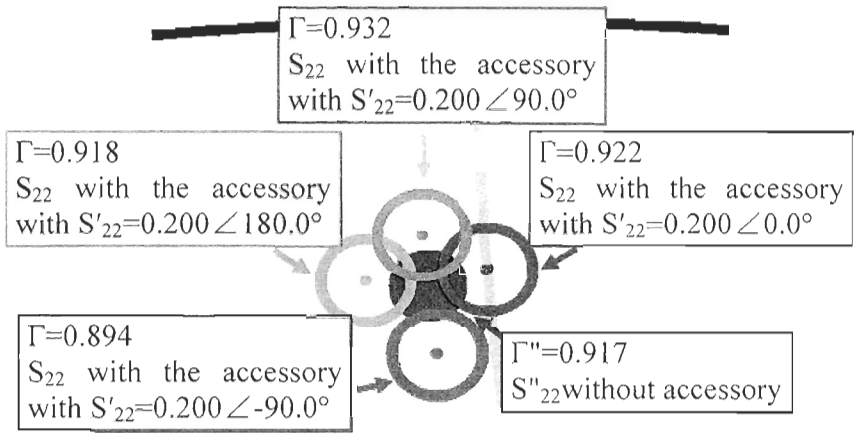


Figure 62 : S''_{22} (filled circle) before adding accessory and S_{22} (hollow circle) after adding the accessory with different phases of S'_{22} on the left side of the source pull tuner

As a 3rd step, in order to see how the accessory effect another S''_{22}, we choose the following calibrated impedance points of source pull tuner: $0.920\angle 180.0°$, $0.928\angle -89.9°$ and $0.929\angle 0.1°$. Same procedure is done for these impedance points as what has been done for $S''_{22}=0.917\angle 90.9°$ in Figure 62. The results are plotted on Smith chart in Figure 63.

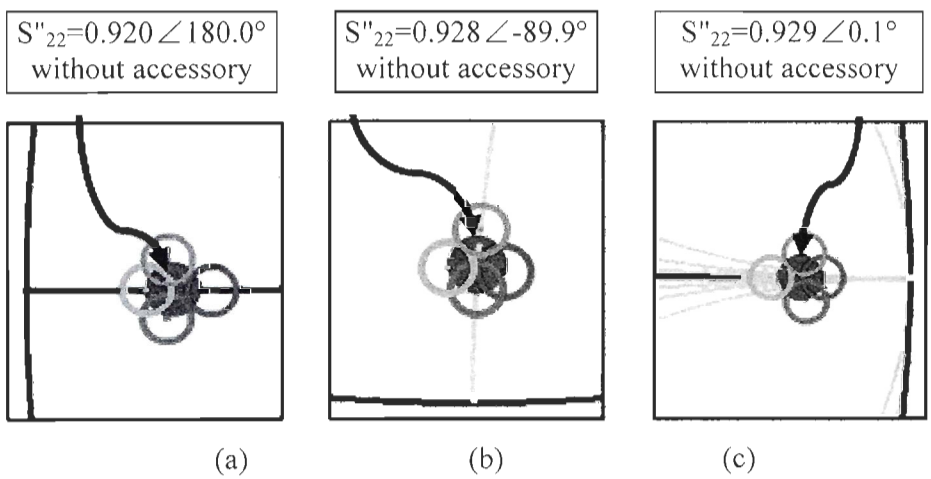


Figure 63 : S_{22} (hollow circle) when the accessory with different S'_{22} is added for $S''_{22}=0.920\angle 180.0°$ (a), $S''_{22}=0.928\angle -89.9°$ (b) and $S''_{22}=0.929\angle 0.1°$ (c)

In Figure 62 and Figure 63, we can see that the Γ of S_{22} could be increased when the phase of S'_{22} of added accessory is similar to the phase of S''_{22} of source pull tuner.

Meanwhile, the Γ of S_{22} could be decreased when there is 180.0° difference between the phase of S'_{22} of the added accessory and the phase of S''_{22}. Therefore, the phase of S'_{22} of the added accessory determines the shifting direction of the calibrated impedance point as shown in Figure 64.

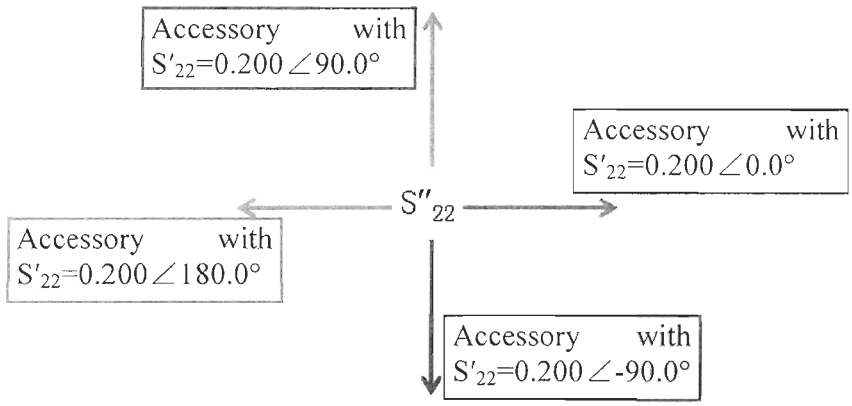


Figure 64 : Effect of the phase of S'_{22} of the accessory

As a 4th step, in order to analyze the effect of the Γ′ of S'_{22} on calibrated impedance point, the Γ′ of S'_{22} is changed from 0.000 to 0.600 with 0.200 step, while the phase of S'_{22} is fixed to 90.0°. Calibrated impedance point S''_{22}=0.917∠90.9° is used. Figure 65 shows the simulated S_{22} result when the Γ′ of S'_{22} is changed from 0.200 to 0.600. The Γ of S_{22} is increased by increasing Γ′ of S'_{22}.

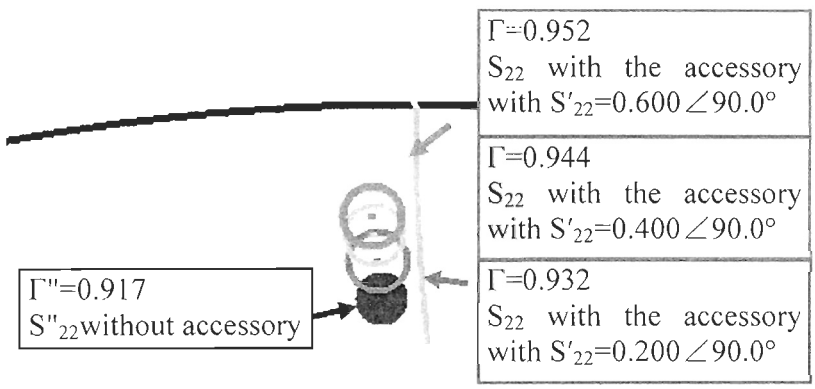


Figure 65 : S''_{22} (filled circle) before adding accessory and S_{22} (hollow circle) after adding the accessory with different Γ′ of S'_{22} on the left side of the source pull tuner

Table 12 summarizes the simulated result for Γ at the DUT reference plane when the Γ′ of S'_{22} changes from 0.000 to 0.600 and the phase of S'_{22} is fixed to 90.0° for $S''_{22}=0.917\angle 90.9°$. As shown in Figure 65 and Table 12, the Γ at the DUT reference plane could be increased more by adding the accessories with higher magnitude of S'_{22}, such as -8 or -4 dB, when the phase of S'_{22} is similar to the phase of S''_{22}. Thus, the magnitude of the accessory's S'_{22} decides the shifting distance as shown in Figure 66.

Table 12 : Simulated results for the Γ of S_{22} when the Γ′ of S'_{22} changes from 0.000 to 0.600 for $S''_{22}=0.917\angle 90.9°$

Γ′ of S'_{22} of accessory	**Magnitude of S'_{22} of accessory (dB)**	**Γ of S_{22} after adding the accessory**	**Increased Γ by the accessory**
0	-50	0.917	0.000
0.2	-14	0.932	0.015
0.4	-8	0.944	0.027
0.6	-4	0.952	0.035

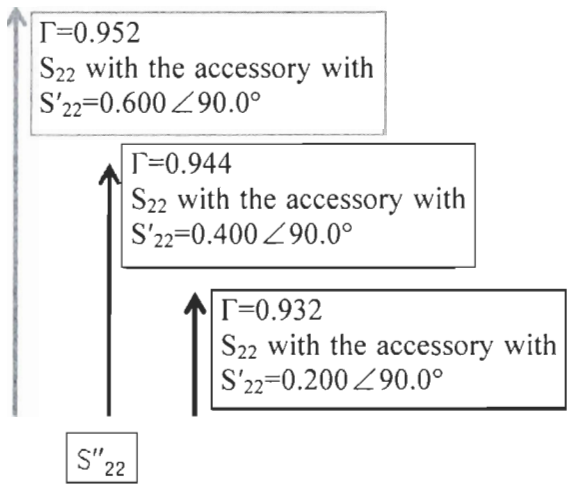


Figure 66 : Effect of the magnitude of S'_{22} of the added accessory

For a contour consisting of 8 calibrated impedance points S''_{22} (dotted circle in Figure 67), after adding an accessory with $S'_{22}=0.600\angle 90.0°$ on the left side of the source pull

tuner, the contour of S_{22} at the DUT reference plane (solid circle in Figure 67) is shifted to the upper direction of 90.0° as shown in Figure 67.

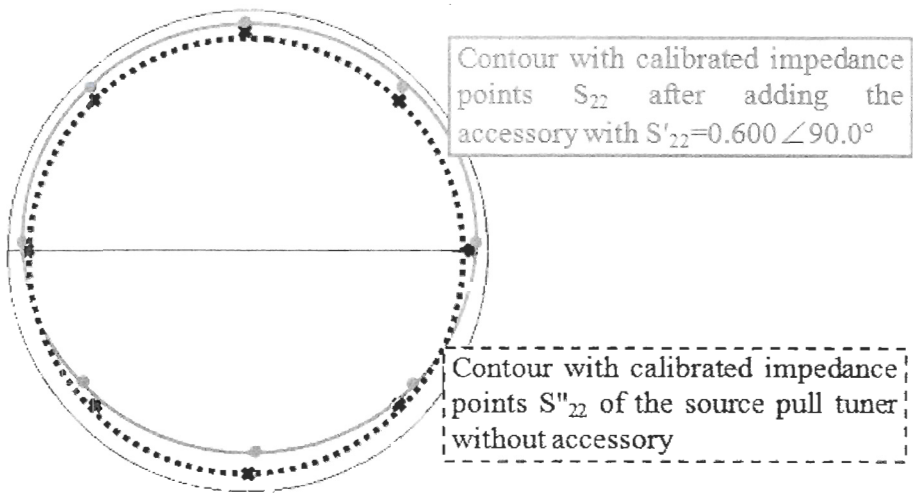
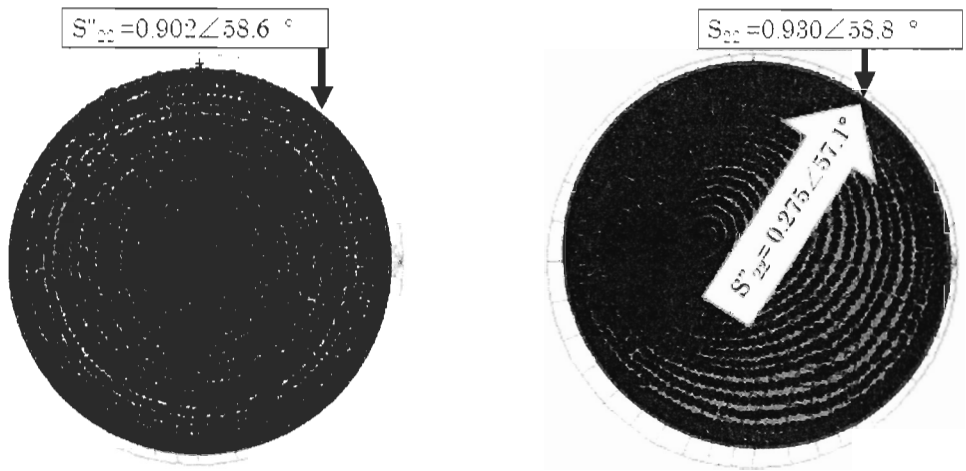


Figure 67 : Contour consisting of 8 calibrated impedance points before (dotted) and after (solid) adding the accessory

In order to evaluate this method, a UTE microwave's CT-4464 isolator with S'_{22}=0.275 ∠57.1° is chosen as the accessory to be added on the left side of the source pull tuner. Figure 68 shows the contour of S_{22} at the DUT reference plane before and after adding this isolator. From Figure 68, we can see that the contour is shifted by the isolator to the direction of 57.1°.

For one calibrated impedance of the source pull tuner S''_{22} =0.902∠58.6° which has similar phase to the phase of S'_{22} of the isolator, the Γ at the transistor reference plane is increased from 0.902 to 0.930 after adding the isolator. Thus, the calibrated impedance contour can be shifted intentionally to increase the maximum Γ at the transistor reference plane by choosing the accessory.



(a) (b)

Figure 68 : Contour of calibrated impedance points before (a) and after (b) adding a UTE microwave CT-4464 isolator

For the load pull tuner, the accessory should be added on the right side of the tuner as shown in Figure 69.

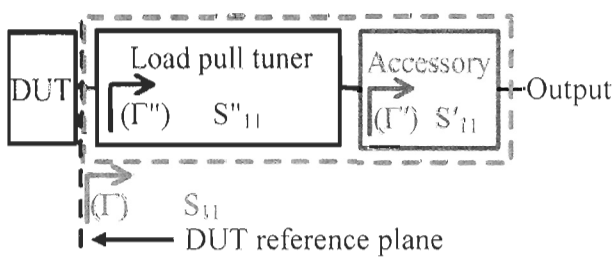


Figure 69 : Setup for the load pull tuner with the accessory

Similar to the source pull tuner, for the added accessory on the right side of the load pull tuner. S_{11} in the DUT reference plane can be expressed as

$$S_{11} = S_{11}^{"} + \frac{S_{21}^{"} S_{12}^{"} S_{11}^{'}}{1 - S_{22}^{"} S_{11}^{'}} \tag{10}$$

where $S"_{11}$, $S"_{22}$, $S"_{12}$ and $S"_{21}$ are the S-parameter of the load pull tuner and S'_{11} is S_{11} of the accessory. According to (10), S'_{11} of the accessory on the right side of the load pull

tuner changes the S_{11} at the DUT reference plane for one fixed calibrated impedance point of the load pull tuner, so the magnitude and phase of S'_{11} affect the shifting distance and direction of load pull tuner's calibrated region. In conclusion, in order to increase Γ of S_{11}/S_{22} with a certain phase at the DUT reference plane for the load/source pull tuner, the phase of S'_{11}/S'_{22} of the chosen accessory should be similar to the phase of target S_{11}/S_{22} and the magnitude of S'_{11}/S'_{22} of the chosen accessory should be higher, such as -8 dB or -4 dB, so that the Γ of S_{11}/S_{22} at the DUT reference plane could be increased more in the desired direction. It is worth noticing that if the phase of S'_{11}/S'_{22} of the chosen accessory has 180° difference from the phase of target S_{11}/S_{22}, the Γ could be reduced. The result in this work and the results obtained by another authors are shown in Table 13.

Table 13 : Published works for increasing the maximum Γ of the passive tuner system

References	Method	Result
(Ghannouchi *et al.*, 2010)	Add passive loop structure	Increase Γ from 0.850 to 0.950 for source pull tuner; Increase Γ from 0.750 to 0.970 for load pull tuner.
(Focus microwaves Inc., 1999 and Maury microwave Inc., 2000; cité par Hashmi *et al.*, 2011)	Pre-matching network	Increase Γ from 0.750 to 0.900 - 0.920
This work	Analyze and choose accessories in the tuner system	Increase Γ from 0.902 to 0.930

3.5 CONCLUSION

In this work, we proposed a novel method which could increase the reflection coefficient Γ of the passive source/load pull tuner by choosing the accessories in the source/load pull tuner system with considering their S-parameters.

The original idea is to analyze the effect of the added accessories on the calibrated region. By the analysis, we found that the calibrated region of the load/source pull tuner

could be shifted by choosing accessories with different magnitudes and phases of S'_{11}/S'_{22}. The phase of S'_{11}/S'_{22} determines the shifting direction. The magnitude of S'_{11}/S'_{22} affects the shifting distance of the Γ. The accessory with higher magnitude of S'_{11}/S'_{22}, such as -4 or -8 dB, should be chosen if more Γ of the passive tuner need to be increased. By this method, the maximum Γ can be increased from 0.902 to 0.930 without adding extra components in the tuner system.

Our contribution in this work is that we proposed a novel method to increase the maximum Γ of the passive tuner system without adding any extra component in the passive tuner system. This novel method can be used to increase the maximum Γ of the passive tuner system by choosing the accessories in the tuner system based on the analysis of the effect of the accessories on the maximum Γ of the passive tuner system.

The publication related to the work in this chapter is referenced as below:

GAO, Shengjie, Zhebin WANG and Chan-Wang PARK. 2012. « Contour method to shift the calibrated region of source/load pull tuners in power amplifier characterization ». In *IEEE Asia-Pacific Microwave Conference.* (Kaohsiung, Taiwan, 4-7 December 2012).

CHAPITRE 4
ANALYSIS AND DESIGN OF THE WIDEBAND BIAS CIRCUIT FOR LTE SIGNAL

4.1 RÉSUMÉ

Dans ce chapitre, une méthode de conception d'un circuit de polarisation à large bande constitué d'une ligne de transmission avec une longueur de λ/4 à haute impédance et un *stub* radial pour l'AP de classe F inverse pour un signal de LTE est proposée. Afin de concevoir un circuit de polarisation pour un signal LTE avec 100 MHz de bande passante, les composants dans le circuit de polarisation, comme la ligne de transmission à haute impédance et *stub* radial, sont analysés et conçus pour atteindre une performance à large bande. L'analyse se concentre sur la façon dont l'impédance de la ligne de transmission et l'angle du *stub* radial changent les paramètres RF du circuit de polarisation, tels que la perte d'insertion, la perte de retour, et l'isolement de RF au port d'entrée DC. Sur la base de cette analyse, le circuit de polarisation est conçu pour offrir un isolement RF maximal au port d'entrée DC, maximiser la perte de retour et minimiser la perte d'insertion dans la bande passante de 100 MHz. Le circuit de polarisation fabriqué peut fournir une perte d'insertion de 0.15 dB, une perte de retour de 41.02 dB, et une isolation RF au port d'entrée DC de 63.59 dB à 3.5 GHz. Dans la bande de fréquences de 3.45 à 3.55 GHz, le circuit de polarisation fabriqué fournit de 0.07 à 0.15 dB de la perte d'insertion, 37.47 à 41.12 dB de perte de retour et 57.87 à 65.52 dB d'isolation RF au port d'entrée DC.

4.2 ABSTRACT

In this chapter, a design method for a wideband bias circuit consisting of a high impedance transmission line and a radial stub for the LTE signal is proposed. In order to design a wideband bias circuit for a 100 MHz LTE signal, the components in the bias circuits, such as the high impedance transmission line and the radial stub, are analyzed and designed to achieve a wideband performance. The analysis focuses on how these components in the bias circuit structure change the RF parameters of the bias circuit in 100 MHz bandwidth, such as the insertion loss, the return loss and the RF isolation to the DC input port. Based on the analysis, the bias circuit is designed to offer higher RF isolation to the DC input port and return loss and lower insertion loss in 100 MHz bandwidth. The fabricated bias circuit can provide 0.15 dB insertion loss, 41.02 dB return loss and 63.59 dB RF isolation to the DC input port at 3.5 GHz. In the frequency range from 3.45 to 3.55 GHz, the fabricated bias circuit provides 0.07-0.15 dB insertion loss, 37.47-41.12 dB return loss and 57.87-65.52 dB RF isolation to the DC input port.

4.3 INTRODUCTION

As introduced in section 1.1.1, the 4G standard, such as LTE or LTE-Advanced requires the PA to support wider bandwidth which is up to 100 MHz. The bias circuit is an important part of a PA. Therefore, in order to achieve an LTE inverse class F PA, a wideband bias circuit is needed. The bias circuit provides DC power for the transistor. A basic biasing network consists of a bypass capacitor and an RF chock is shown in Figure 70 (Bahl, 2009 : 514). The RF chock is used to have high impedance at the operating frequency to block the RF signal from the leaking through the biasing circuit to the DC source. What's more, when the RF chock presents high impedance to the matching network, the effect of the bias circuit is negligible. The bypass capacitor should present a short circuit (low impedance) at the operating frequency (Bahl, 2009 : 514).

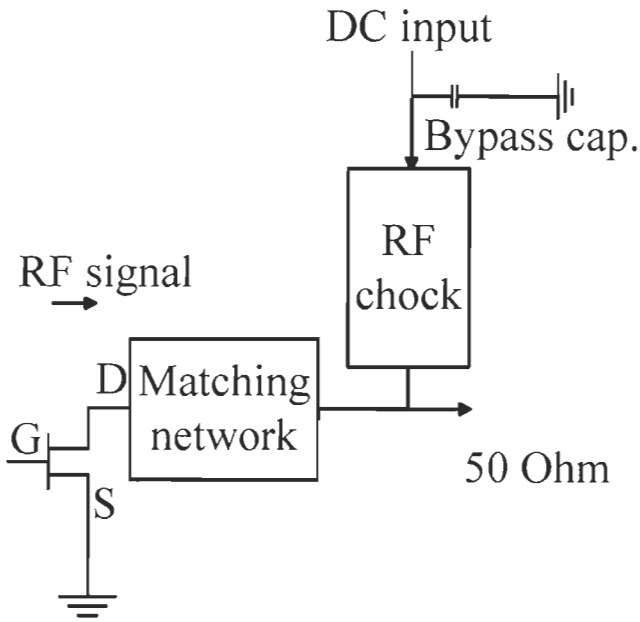


Figure 70 : Basic structure of bias circuit

The insertion loss, return loss and RF isolation to the DC input port are three important factors for the bias circuit. Less insertion loss and more return loss could reduce the RF power dissipation in the bias circuit. High RF isolation to the DC input port could prevent oscillation of PA (Wei *et al.*, 2007).

Baylis *et al.* shows a procedure to design the bias circuit that used an inductor in the RF chock (Baylis *et al.*, 2006). They have achieved less than 1 dB insertion loss, more than 15 dB return loss and RF isolation to the DC input port in the frequency range from 1 GHz to 2 GHz.

Instead of using inductor and bypass capacitor, Wei *et al.* proposed a high impedance $\lambda/4$ microstrip transmission line and a microstrip radial stub are used to be a RF chock and a bypass capacitor in the bias circuit, respectively (Wei *et al.*, 2007). They have achieved less than 0.40 dB insertion loss, more than 20.00 dB return loss in the frequency range from 7 GHz to 9 GHz.

The objective in this chapter is to design a wideband bias circuit for a LTE inverse class F PA at 3.5 GHz. The expected RF performances of the designed wideband bias circuit are: a) at least 30 dB return loss and RF isolation to the DC input port at 3.5 GHz in 100 MHz bandwidth; b) less than 0.2 dB insertion loss at 3.5 GHz in 100 MHz bandwidth.

In this work, we choose the bias circuit structure consisting with a high impedance λ/4 (at 3.5 GHz) microstrip transmission line and a microstrip radial stub. In the next section, the λ/4 microstrip transmission line and the microstrip radial stub in the bias circuit are analyzed. Based on the analysis, the bias circuit is designed to minimize the insertion loss while maximize the RF isolation to the DC input port and return loss at 3.5 GHz in 100 MHz bandwidth.

4.4 PROPOSE METHOD OF DESIGNING THE WIDEBAND BIAS CIRCUIT FOR THE LTE SIGNAL

In this section, the method of designing the bias circuit consisting with a high impedance λ/4 microstrip transmission line and a microstrip radial stub is presented. As a first step, this bias circuit is analyzed and designed in the ADS schematic. Then, based on the analysis and design in ADS schematic, the layout of the bias circuit is simulated and adjusted by Momentum simulation. At last, this bias tee is fabricated based on the layout in Momentum simulation and the measured results are compared with the Momentum simulation result.

4.4.1 Design in ADS schematic

In ADS schematic, the basic structure of bias circuit consisting of a λ/4 (at 3.5 GHz) microstrip transmission line TL1 terminated by microstrip radial stub is shown in Figure 71 (Mongia *et al.*, 2007). TL2 and TL3 are the 50 Ω main line for passing the LTE signal.

Term 1 and term 2 are the input and output port for the signal. Term 3 is the DC input. By considering that the bias circuit should be connected with DC power supply and extra bypass capacitor may be needed in the bias circuit empirically, TL4 is added between the radial stub and DC power input port. The radial stub is used to provide a RF grounding (low impedance) environment for the bias circuit as a bypass capacitor (Giannini *et al.*, 1986).

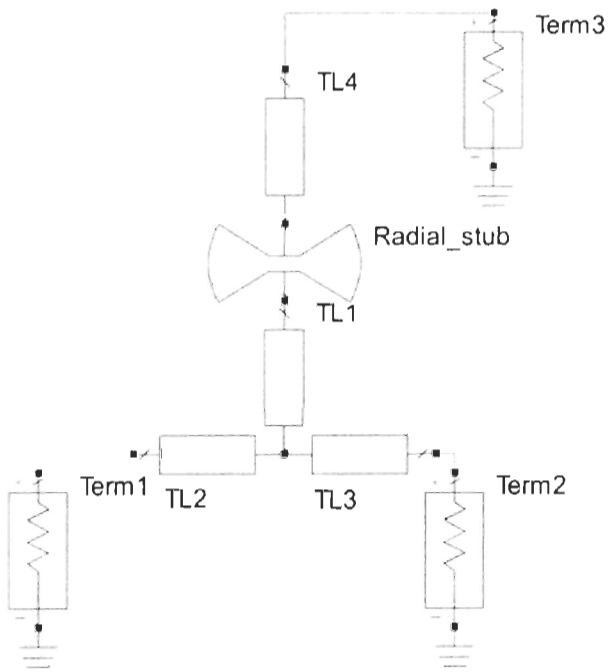


Figure 71 : Proposed structure of bias circuit in ADS schematic

The first step is to determine the radius and angle of radial stub by simulating the radial stub alone as shown in Figure 72. The objective is to achieve low impedance (≈0 Ω) at 3.5 GHz. The angle of the radial stub is changed from 50° to 90° while the radius of the radial stub is optimized to provide low impedance at 3.5 GHz.

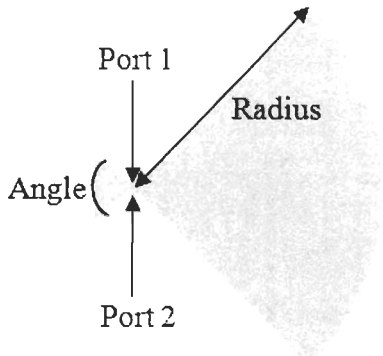


Figure 72 : Structure of the radial stub

The ADS simulation result in Figure 73 shows that larger angle provides lower impedance at 3.5 GHz in 100 MHz bandwidth. Hence, 90° is chosen for the angle of the radial stub. The radial stub with 90° angle and 475 mil radius could offer 40.36 dB suppression and 0.24 Ω impedance at 3.5 GHz by ADS simulation. (1 mil = 0.001 inch)

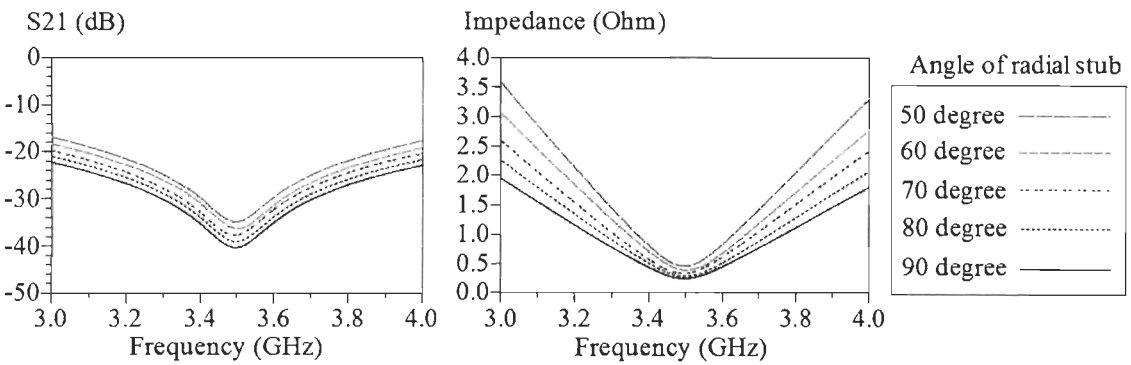


Figure 73 : Simulated results with different radial stub angles

As a second step, the effect of the impedance of λ/4 TL1 on the S-parameter of bias circuit is analyzed after fixing the angle and radius of the radial stub to 90° and 475.00 mil, respectively. Based on (Bahl, 2009 : 514), high impedance λ/4 TL1 should be used to minimize the effect of the bias circuit for reducing RF leakage through the bias circuit. To analyze the effect of the impedance of λ/4 TL1, the impedance of TL1 in Figure 71 is varied from 25 Ω to 100 Ω with λ/4 electrical length at 3.5 GHz. The impedance of main

line TL2 and TL3 in Figure 71 is 50 Ω at 3.5 GHz. With considering mounting the bias circuit on a metal base after fabrication, the lengths of TL2 and TL3 are fixed to 535.41 mil and 700.00 mil, respectively, to fit the dimension of the metal base. The ADS simulation result in Figure 74 shows that the RF isolation to the DC source is increased, while the insertion loss and the return loss are reduced by increasing the impedance of TL1 from 25 Ω to 100 Ω. Hence, 100 Ω is chosen. For the structure in Figure 71, by ADS simulation in schematic, the RF isolation to the DC source is 58.36 dB and the insertion loss is 0.01 dB with 64.38 dB return loss at 3.5 GHz. In 100 MHz bandwidth, the RF isolation to the DC source is more than 55.00 dB and the insertion loss is 0.01 dB with more than 50.00 dB return loss.

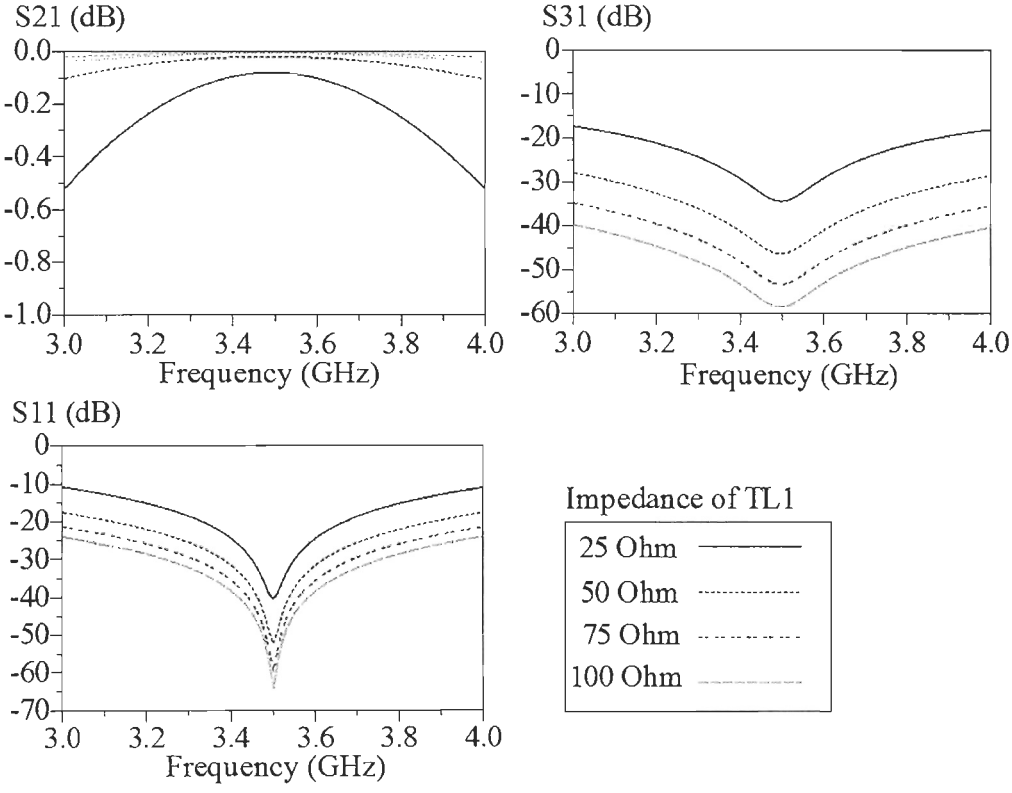
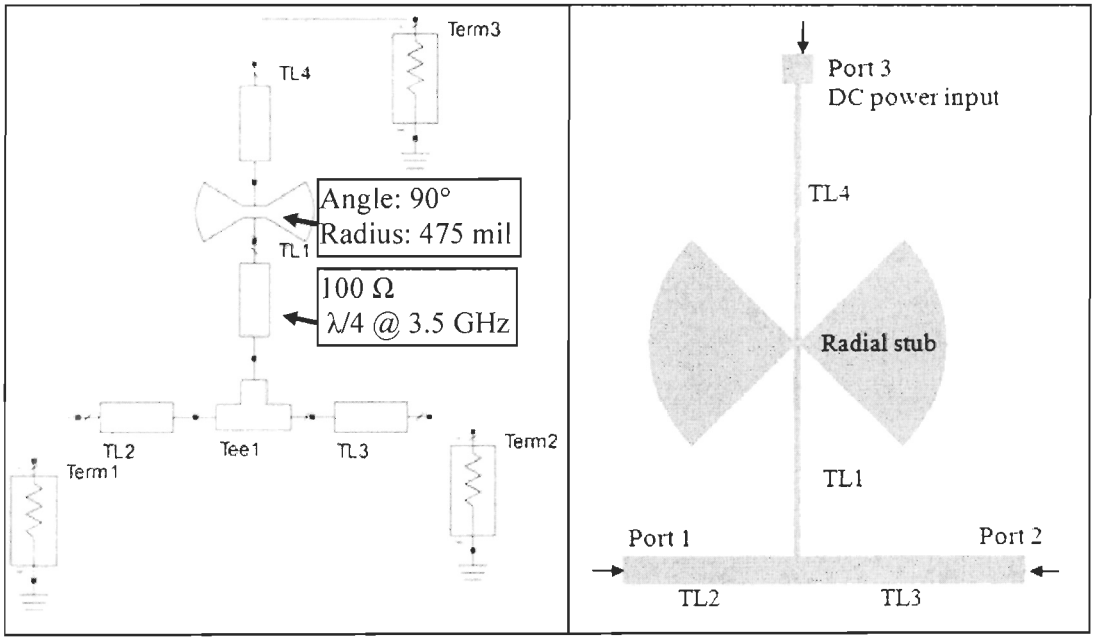


Figure 74 : Simulated results with different characteristic impedances of TL1

By the ADS simulation in schematic, TL4 does not affect the S_{21}, S_{11} and S_{31} of the bias circuit when the impedance of TL1, angle and radius of radial stub are fixed to the values found in the previous steps (100 Ω TL1 with λ/4 electrical length at 3.5 GHz, 90° angle and 475.00 mil radius for radial stub), so the length of TL4 is chosen to be fixed to 800.00 mil. In order to fabricate this bias circuit, the structure of the bias circuit is proposed to be designed as shown in the following figure.



(a) (b)

Figure 75 : Proposed structure (a) and layout (b) for the fabrication of bias circuit

The substrate Rogers RT/duroid 5870 with 31 mil substrate thickness and 17 μm metal thickness is used. Calculated by the utility "LineCalc" in ADS 2011.10, the width and length of 100 Ω λ/4 microstrip line TL1 with Rogers 5870 substrate is 25.28 mil and 623.04 mil, respectively. The width of the 50 Ω main line TL2 and TL3 is 91.02 mil. The dimensions of the microstrip components in the designed bias tee are listed in Table 14.

Table 14 : Dimensions of the microstrip components used in the bias circuit

Components	Dimension (mil)
TL1	Length: 623.04, Width: 25.28
TL2	Length: 535.41, Width: 91.02
TL3	Length: 700.00, Width: 91.02
TL4	Length: 800.00, Width: 25.28
Radial stub	Angle: 90°, Radius: 475.00
Tee1	Length: 25.28, Width: 91.02

With these dimensions, the ADS simulation result of the structure in Figure 75 (a) is shown in Figure 76. The result shows that S_{11}=-37.37 dB, S_{21}=-0.01 dB and S_{31} = -57.73 dB at 3.5 GHz. In 100 MHz, S_{11} is between -34.25 and -42.28 dB, S_{21} is 0.01 dB and S_{31} is between -55.45 and -57.72 dB.

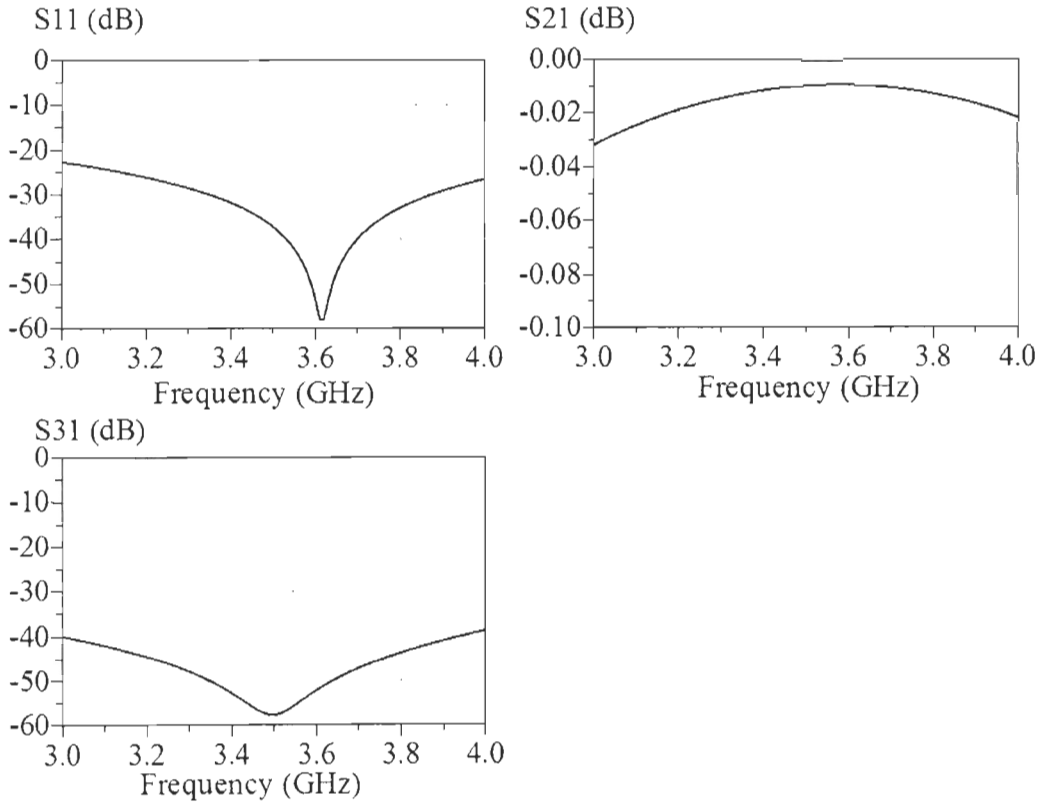


Figure 76 : ADS simulation result of the bias circuit

4.4.2 Design in ADS Momentum simulation

After finishing the design in ADS schematic, the bias circuit is simulated and adjusted by Momentum simulation. Momentum simulation is a 3D planar electromagnetic (EM) simulator that enables RF and microwave designers to significantly expand the range and accuracy of their passive circuits. The ability to consider real-world design geometries when simulating coupling and parasitic effects makes Momentum an indispensable tool for customized passive circuit design (Agilent Inc., 2011b). Compared with the simulation in schematic, the results obtained by Momentum are more accurate, because it considers the parasitic coupling and radiation in the passive circuit.

The accuracy of Momentum simulation could be improved by increasing mesh number (Agilent Inc., 2011b). However, the Momentum simulation with more mesh number requires more time. Therefore, as a first step, a parametric study should be done to determine the mesh number in Momentum simulation for obtaining accurate result within reasonable time. For the layout of the bias circuit in Figure 75 (b), the mesh number is changed from 20 to 100 with 11 GHz mesh frequency. Table 15 summarizes the Momentum simulation results of the bias circuit in Figure 75 (b) at 3.5 GHz with different mesh and their corresponding simulation time. From Table 15, we can see that, when the mesh number is more than 60, the difference in S_{11} of the bias circuit is within 0.82 dB, the difference in S_{21} is within 0.01 dB, the difference in S_{31} is within 0.14 dB. Thus, by considering the simulation time and accuracy, 60 mesh is chosen.

Table 15 : Momentum simulation results of the bias circuit layout in Figure 75 (b) at 3.5 GHz with different mesh number and the corresponding simulation time

Mesh	S_{11} (dB)	S_{21} (dB)	S_{31} (dB)	Simulation time
20	-36.34	-0.02	-50.47	30 seconds
40	-32.32	-0.03	-51.49	75 seconds
60	-34.35	-0.03	-51.30	3 minutes
80	-33.59	-0.02	-51.29	7 minutes
100	-34.41	-0.03	-51.16	15 minutes

By Momentum simulation with 60 mesh, the length of TL1 and radius of the radial stub are adjusted to increase the return loss and minimize the insertion loss, while maintaining S_{31} less than -30 dB. After adjusting by Momentum simulation, the dimensions of the microstrip components in the bias tee in Figure 75 (b) are listed in Table 16. The Momentum simulation results are shown in Figure 77.

Table 16 : Dimensions of the microstrip components in the bias circuit designed by Momentum simulation

Components	Dimension (mil)
TL1	Length: 654.00, Width: 25.28
TL2	Length: 535.41, Width: 91.02
TL3	Length: 700.00, Width: 91.02
TL4	Length: 800.00, Width: 25.28
Radial stub	Angle: 90°, Radius: 466.50
Tee1	Length: 25.28, Width: 91.02

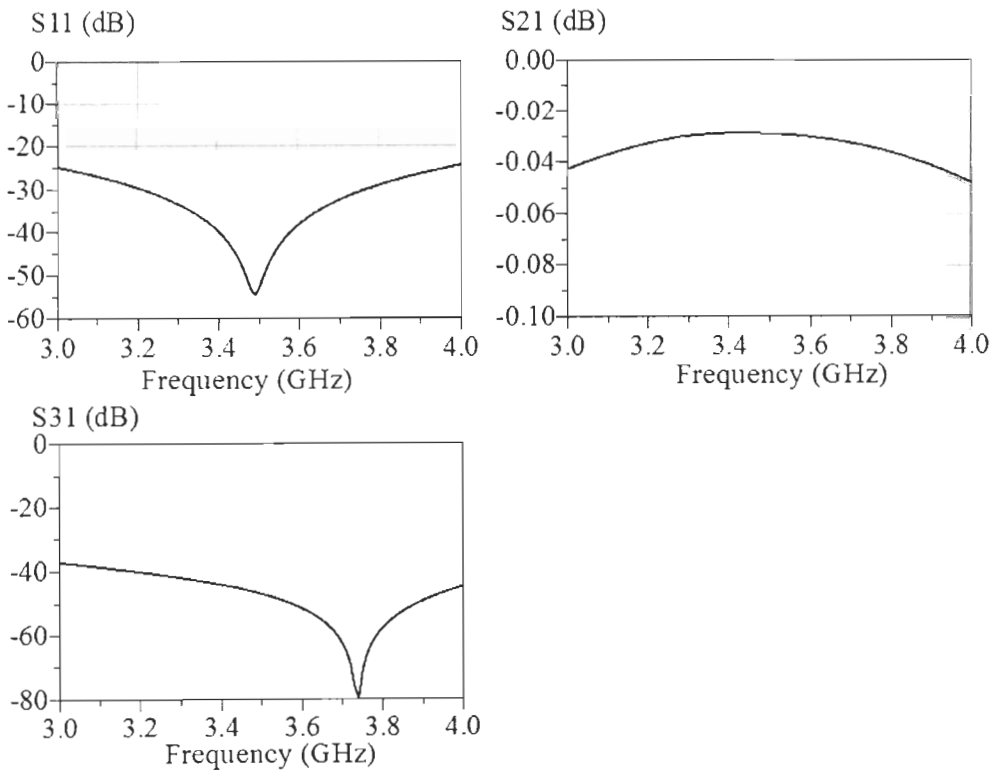


Figure 77 : Momentum simulation result of the bias circuit with 60 mesh

In Figure 77, S_{11}=-56.35 dB, S_{21}=-0.02 dB and S_{31}=-46.98 dB at 3.5 GHz. In 100 MHz bandwidth, S_{11} is between -43.85 and -57.24 dB, S_{21}=-0.02 dB and S_{31} is between -45.36 and -48.94 dB. Thus, this bias circuit satisfies the objective (S_{11}/S_{31}<-30 dB and S_{21}>-0.2 dB).

4.5 FABRICATION AND MEASUREMENT OF THE WIDEBAND BIAS CIRCUIT FOR LTE SIGNAL

The bias circuit is fabricated with Rogers RT/duroid 5870 substrate with 31 mil substrate thickness and 17 μm metal thickness. The fabricated bias circuit is shown in Figure 78. The measured result compared with Momentum simulation result is shown in Figure 79 and Table 17.

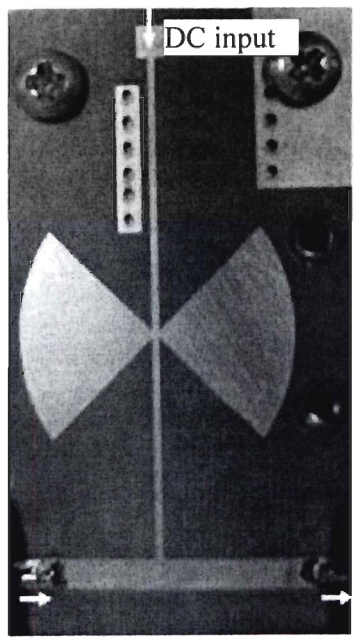


Figure 78 : Fabricated bias circuit

The measured insertion loss is 0.15 dB, the return loss is 41.02 dB and the RF isolation to the DC input port is 63.59 dB at 3.5 GHz. The tendency of the measured bias

circuit's S-parameter result is similar to the Momentum simulation result. In 100 MHz bandwidth, the measured insertion loss is less than 0.18 dB, the measured return loss is more than 30.00 dB, and the measured RF isolation to the DC input port is more than 57.00 dB.

Table 17 : Measured and simulated results of the bias circuit at 3.5 GHz

	S_{11} (dB)	S_{21} (dB)	S_{31} (dB)
Measured result	-41.02	-0.15	-63.59
Simulation result	-56.35	-0.02	-46.98

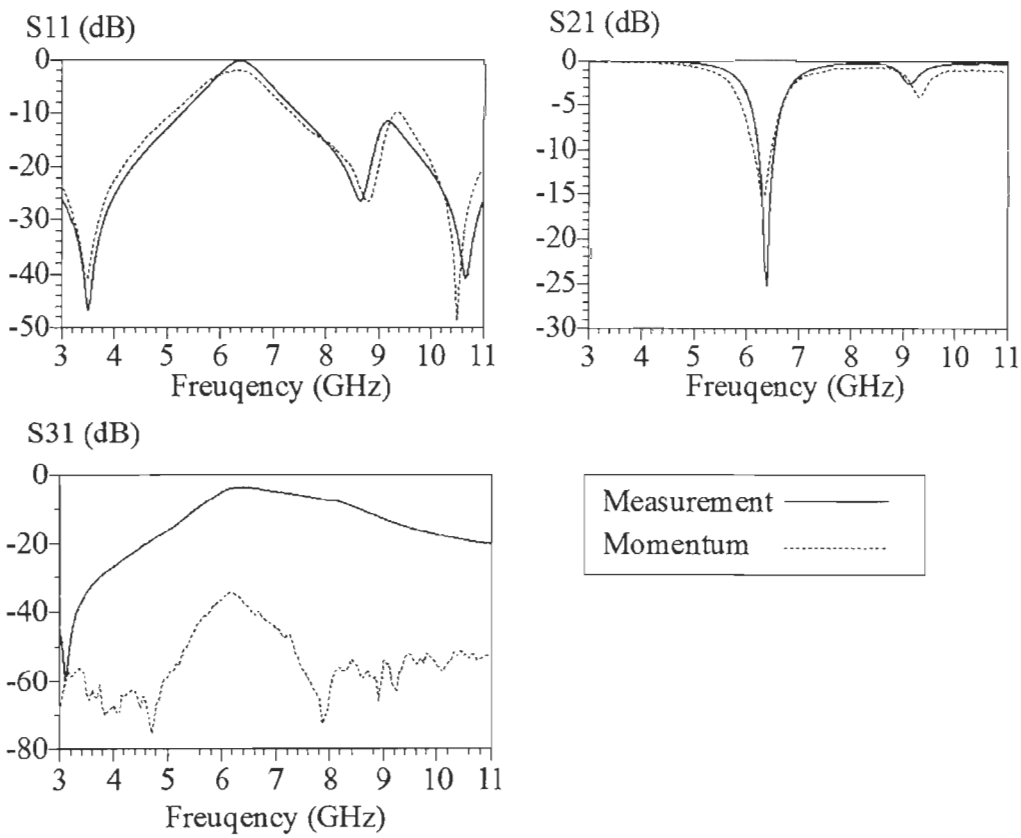


Figure 79 : Comparison between measured result and Momentum simulation result of the bias circuit

In the frequency range from 3.45 to 3.55 GHz, the fabricated bias circuit provides 0.07-0.15 dB insertion loss, 37.47-41.12 dB return loss and 57.87-65.52 dB RF isolation to

the DC input port. The measured results are compared with the results obtained by other authors in Table 18. From this table, we can see that the bias circuit fabricated in this work provides the lowest insertion loss and highest return loss and RF isolation to the DC input port.

Table 18 : Published works for designing bias circuit

Reference	S_{11} (dB)	S_{21} (dB)	S_{31} (dB)
(Baylis *et al.*, 2006)	<-15.00 @ 1-2 GHz	>-1.00 @ 1-2 GHz	<-15.00 @ 1-2 GHz
(Wei *et al.*, 2007)	<-20.00 @ 7-9 GHz	>-0.40 @ 7-9 GHz	N/A
This work	<-37.47 @ 3.45-3.55 GHz	>-0.15 @ 3.45-3.55 GHz	<-57.87 @ 3.45-3.55 GHz

4.6 CONCLUSION

In this work, a method of designing a wideband bias circuit for the LTE signal is proposed. With this proposed method, we analyzed, designed and fabricated a bias circuit consisting of a 100 Ω λ/4 microstrip transmission line and a microstrip radial stub. The impedance of λ/4 microstrip transmission line and the angle of radial stub in the bias circuit are analyzed to increase the bandwidth of the RF isolation to the DC input port and the return loss and to reduce the insertion loss of the bias circuit. The fabricated bias circuit shows that 0.15 dB insertion loss, 41.02 dB return loss, and 63.59 dB RF isolation to the DC input port could be measured at 3.5 GHz. In the frequency range from 3.45 to 3.55 GHz, the fabricated bias circuit provides 0.07-0.15 dB insertion loss, 37.47-41.12 dB return loss and 57.87-65.52 dB RF isolation to the DC input port.

The contribution in this work is that we proposed a method for designing a wideband bias circuit for 100 MHz bandwidth LTE signal by analyzing the components in the bias circuit, such as the λ/4 microstrip transmission line and the microstrip radial stub. With this method, we could achieve a bias circuit with an insertion loss less than 0.15 dB in 100 MHz bandwidth, while the RF isolation to the DC input port and return loss are more than 57.87 dB and 37.47 dB, respectively.

CHAPITRE 5
EVALUATION OF THE CHARACTERIZATION RESULTS OBTAINED BY THE MULTI-HARMONIC TUNER SYSTEM AND BY THE SIMULATION

5.1 RÉSUMÉ

Dans ce chapitre, les AP classe F inverse sont conçus sur la base des résultats de la caractérisation du chapitre 2. Les résultats mesurés des APs fabriqués sont utilisés pour évaluer les résultats de la caractérisation obtenus. La procédure de la conception des circuits d'adaptation d'impédance d'APs classe F inverse est proposée. Dans les circuits d'adaptation d'impédance des APs classe F inverse pour le signal 1-ton, des *stubs* droits avec une longueur de $\lambda/4$ à 7 et 10.5 GHz sont utilisés pour supprimer les $2^{ème}$ et $3^{ème}$ harmoniques. Après la fabrication, nous avons constaté que les fréquences supprimées par le *stub* avec une longueur de $\lambda/4$ sont décalés parfois. Pour pallier ce problème, des *stubs* radiaux sont utilisés. Les *stubs* augmentent la largeur de bande de la suppression de $2^{ème}$ et $3^{ème}$ harmoniques, comparativement aux *stubs* droits. L'effet des paramètres du *stub* radial est analysé par rapport à la largeur de bande de suppression. Sur la base de cette analyse, les circuits d'adaptation d'impédance avec le *stub* radial sont conçus et fabriqués pour l'AP de classe F inverse pour un signal de LTE. Les résultats mesurés des APs de classe F inverse fabriqués pour le signal 1-ton et le signal LTE sont analysés et comparés avec les résultats de la caractérisation obtenus au chapitre 2 d'identifier la meilleure méthode de caractérisation est déterminée.

5.2 ABSTRACT

In this chapter, inverse class F PAs are designed and fabricated based on the results of the characterization in chapter 2. The measured results of the fabricated PAs will be used to evaluate the results of the characterizations. The procedure for designing the input and output impedance matching networks for these inverse class F PAs is proposed. In the matching network circuits for the 1-tone inverse class F PAs, the straight λ/4 stubs at 7 and 10.5 GHz are used to suppress the 2nd and 3rd harmonic frequencies. After the fabrication of the matching network with straight λ/4 stubs, we found that the frequencies suppressed by the straight λ/4 stubs are sometimes shifted. To counter this problem, microstrip radial stubs are used. These stubs increase the bandwidth of the suppression at the 2nd and 3rd harmonic frequencies, comparatively to straight ones. The effect of the parameters of the radial stub is analyzed in terms of the bandwidth of the suppression. Based on the analysis, the impedance matching network circuits with the radial stub are designed and fabricated for the LTE inverse class F PA. The measured results of the fabricated 1-tone and LTE inverse class F PAs are analyzed and compared with the characterization results obtained in chapter 2 to identify the best characterization method.

5.3 INTRODUCTION

Impedance matching network is an essential part of an amplifier design, because amplifiers must be properly terminated at both the input and output of the transistor to achieve desired performance, such as 40 dBm output power or maximum PAE (Gonzalez, 1996 : 112). In order to evaluate the characterization results obtained by the multi-harmonic tuner system and by the simulation in chapter 2, the impedance matching networks of the inverse class F PA should be well designed to match the impedances found in the characterizations. As mentioned in chapter 2, the 2nd and 3rd harmonic should be well

suppressed to achieve the high PAE. Therefore, the question is how to suppress the harmonic frequencies in an inverse class F PA.

In (Abe *et al.*, 2008), the parallel LC resonators are used to suppress the harmonic frequencies in an inverse class F PA with GaN HEMT transistor. Measured maximum PAE 76.30% is founded at 879 MHz when the output power is 30.00 dBm. However, the authors mentioned that the chip components (inductors and capacitors) used in the circuits need to be adjusted after fabrication to well suppress the harmonic frequencies due to the parasitic elements of the chip components. Therefore, this method cannot be adopted since the first-pass design methodology is our objective.

In (Helaoui *et al.*, 2009), the straight λ/4 microstrip line stubs are used in the input and output impedance matching network to suppress harmonic frequencies. The fabricated PA with CGH40010 transistor shows that the maximum PAE 81.30% is founded at 1.01 GHz when the output power is 39.70 dBm.

In (Moon *et al.*, 2012b), the straight λ/4 microstrip line stubs are also used to suppress the harmonic frequencies. The fabricated PA with CGH40006 transistor shows that the maximum PAE 80.10% is founded at 3.48 GHz when the output power is 38.40 dBm and gain is 14.40 dB.

In (Wang *et al.*, 2012b), the microstrip radial stubs are used to suppress harmonic frequencies in wider bandwidth compared with straight λ/4 stubs. The fabricated PA with CGH40010 transistor shows that the maximum PAE 80.52% is founded at 2.14 GHz when the output power is 40.53 dBm.

Based on the researches mentioned above, the straight λ/4 microstrip line stub is used to suppress the harmonic frequencies in an inverse class F PA. The objective in this chapter is to evaluate the characterization results obtained by the multi-harmonic tuner system and by the simulation in chapter 2. To do that, the input and output matching networks for the inverse class F PAs should be designed to match the impedances at 3.5 GHz, 7 GHz and 10.5 GHz which obtained in the characterizations in chapter 2. The impedances at 3.5 GHz,

7 GHz and 10.5 GHz chosen in the 1-tone characterization by the source & load pull simulation in ADS and the impedances chosen in the 1-tone and LTE characterization by the multi-harmonic source & load pull tuner system are summarized in Table 19.

Table 19 : Impedances chosen in the 1-tone characterization by the source & load pull simulation in ADS with method no. 1/no. 2 and impedances chosen in the 1-tone and LTE characterization by the multi-harmonic source & load pull tuner system

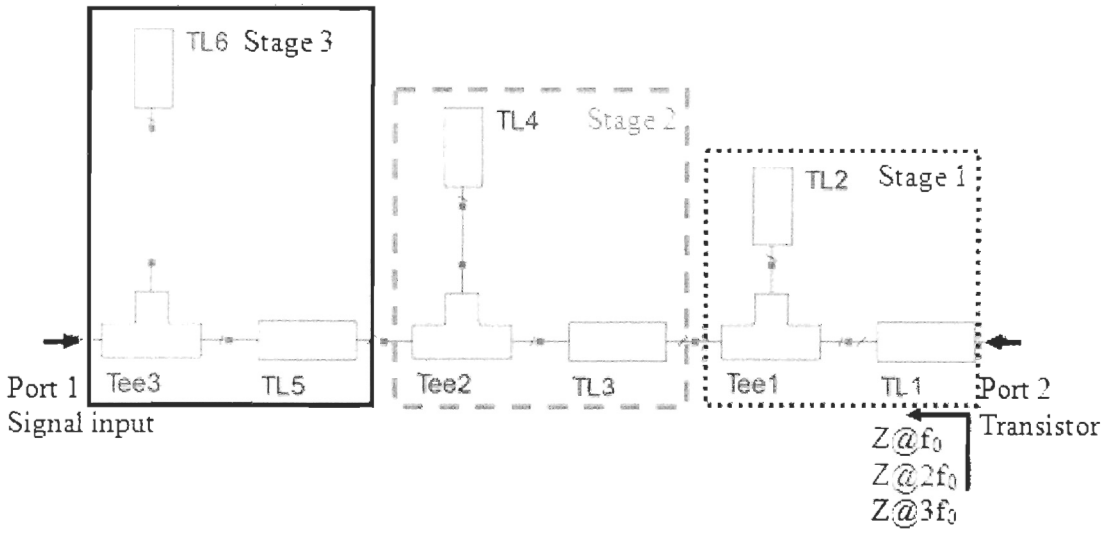
	1-tone characterization results by simulation (method no. 1)	**1-tone characterization results by simulation (method no. 2)**	**1-tone characterization results by multi-harmonic source & load pull tuner**	**LTE characterization results by multi-harmonic source & load pull tuner**
Load imp. @ 3.5 GHz	0.566∠161.7°	0.705∠160.9°	0.603∠165.5°	0.603∠165.5°
Load imp. @ 7 GHz	1.000∠-178.0°	1.000∠144.0°	0.938∠146.1°	0.923∠-166.6°
Load imp. @ 10.5GHz	1.000∠132.0°	1.000∠-172.0°	0.918∠42.6°	0.929∠86.1°
Source imp. @ 3.5 GHz	0.941∠-151.8°	0.941∠-151.8°	0.892∠-151.7°	0.818∠-148.2°
Source imp. @ 7 GHz	1.000∠28.0°	1.000∠0.0°	0.900∠-38.5°	0.929∠147.5°
Source imp. @ 10.5GHz	1.000∠-135.0°	1.000∠180.0°	0.880∠-68.6°	0.919∠94.8°

In section 5.3, a structure of matching network with the straight λ/4 microstrip line stub is proposed to match these impedances found in the 1-tone characterizations by the simulation and by the multi-harmonic tuner system. In section 5.4, the fabricated 1-tone inverse class F PAs are measured, analyzed and compared with the 1-tone characterization results in chapter 2. In section 5.5, a structure of matching network with the microstrip radial stub is proposed to match the impedances found in the LTE characterization by the multi-harmonic tuner system. In section 5.6, the fabricated LTE inverse class F PAs are measured, analyzed and compared with the LTE characterization result in chapter 2 in order to identify the best characterization method is determined.

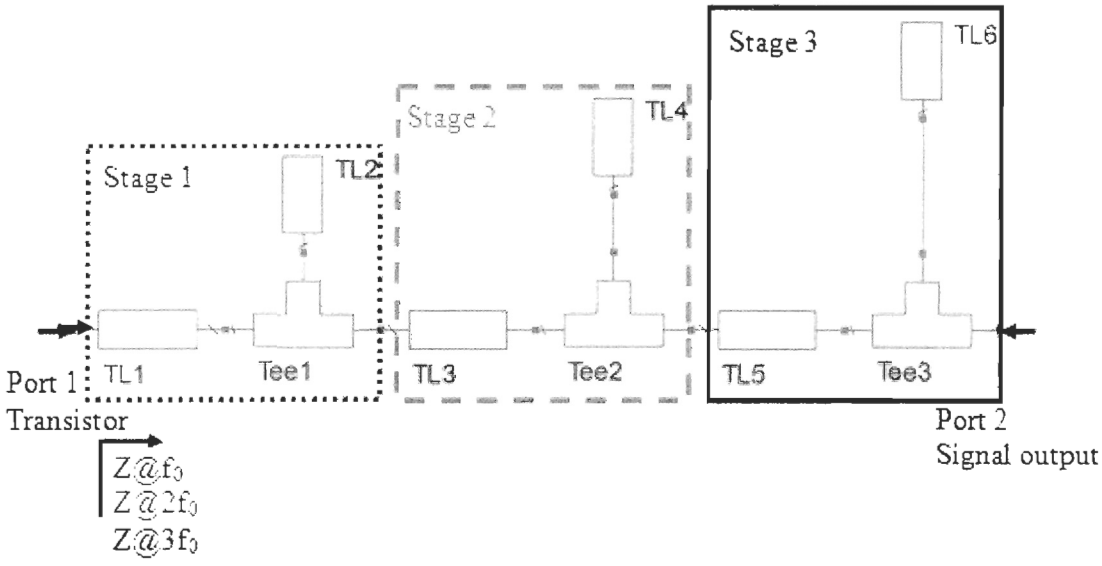
5.4 PROPOSED STRUCTURE OF THE MATCHING NETWORK FOR THE 1-TONE INVERSE CLASS F PA

In order to evaluate the 1-tone characterization results obtained by the multi-harmonic tuner system and by the simulation in chapter 2, a structure of the impedance matching network circuits for the 1-tone inverse class F PAs is presented in this section.

The input and output matching network structures (Helaoui *et al.*, 2009) shown in Figure 80 are adopted for the 1-tone inverse class F PAs. The 50 Ω straight microstrip line stubs (TL2 and TL4) and the microstrip transmission lines in series (TL1 and TL3) in stage 1, 2 are used to suppress the 2^{nd} and 3^{rd} harmonic frequencies and move the impedances at the 3^{rd} and 2^{nd} harmonic frequencies to the target impedances. Impedance at 3.5 GHz is controlled at the stage 3. The bias circuit designed in chapter 4 is added on the left side of the input matching network and on the right side of the output matching network. Because the RF chock in this bias circuit presents high impedance to the matching network, the bias circuit is negligible (Bahl, 2009 : 514). Based on the structures shown in Figure 80, the input and output matching network circuits designed based on the characterization results obtained by the simulation with method no. 1 is shown in section 5.3.1. The input and output matching network circuits designed based on the characterization results obtained by the simulation with method no. 2 is shown in section 5.3.2. The input and output matching network circuits designed based on the characterization results obtained by the multi-harmonic source & load pull tuner system is shown in section 5.3.3.



(a)



(b)

Figure 80 : Proposed structure of the input (a) and output (b) matching network for the 1-tone inverse class F PA

The procedure of designing the matching network is described as follows:

1. Determine by Momentum simulation the length of TL2 in stage 1 to suppress the 3^{rd} harmonic.

2. Determine by Momentum simulation the lengths of TL1 in stage 1 to achieve the target phase of the impedance at the 3rd harmonic frequency.

3. Determine by Momentum simulation the length of TL4 in stage 2 to suppress the 2nd harmonic.

4. Determine by Momentum simulation the lengths of TL3 in stage 2 to achieve the target phase of the impedance at the 2nd harmonic frequency.

5. Determine by Momentum simulation the length of TL5 and TL6 in stage 3 to achieve the target impedance at the fundamental frequency.

The objective of the 1-tone input and output matching networks is to match the source and load impedances at the fundamental, 2nd and 3rd frequencies obtained by the 1-tone source & load pull tuner characterizations in chapter 2. These impedances are listed in Table 19. For the matching network, a parametric study is also done to determine the mesh number in Momentum simulation for obtaining accurate results of the matching network circuits. As a first step of this parametric study, an input matching network is designed by Momentum simulation with 100 mesh based on the 1-tone characterization result obtained by the source & load pull simulation with method no. 1. The used substrate is Rogers RT/duroid 5870 substrate with 31 mil substrate thickness and 35 μm metal thickness. The dimensions of the transmission lines in this input matching network are summarized in Table 20.

Table 20 : The dimensions of the transmission lines in the input matching network designed based on the 1-tone characterization result obtained by the source & load pull simulation with method no. 1

	TL1	**TL2**	**TL3**	**TL4**	**TL5**	**TL6**	**Tee1**	**Tee2**	**Tee3**
Length (mil)	312.30	183.80	279.00	287.50	108.30	549.20	90.17	90.17	90.17
Width (mil)	90.17	90.17	90.17	90.17	90.17	90.17	90.17	90.17	90.17

As a second step, this input matching network circuit is re-simulated by Momentum simulation with the mesh changed from 40 to 100 (11 GHz mesh frequency). Table 21 shows the impedances at 3.5 GHz, 7 GHz and 10.5 GHz obtained by Momentum simulation for the input matching network with different mesh. We can see that, by increasing values of mesh above 60, the difference in magnitude of the impedances is within 0.005, the difference in phase of the impedances is within 0.7°. By considering the accuracy of Momentum simulation and simulation time, 60 mesh is chosen. Thus, to design the input and output impedance matching circuits by Momentum simulation, 60 mesh is chosen to determine the dimension of the transmission lines in stage 1, 2 and 3.

Table 21 : Simulation results by Momentum simulation with different mesh number for the input matching network (designed based on the 1-tone characterization result obtained by the simulation method no. 1)

Mesh	Imp. @ 3.5 GHz	Imp. @ 7 GHz	Imp. @ 10.5 GHz	Simulation time
20	0.941∠-151.4°	0.979∠27.8°	0.928∠-135.0°	1 minute
40	0.941∠-151.3°	0.979∠28.0°	0.927∠-135.0°	1.5 minute
60	0.942∠-151.8°	0.979∠27.7°	0.928∠-135.9°	4 minutes
80	0.943∠-152.3°	0.982∠27.6°	0.933∠-136.2°	9 minutes
100	0.944∠-152.5°	0.980∠27.4°	0.930∠-135.9°	20 minutes

5.4.1 Design of the matching network for the 1-tone characterization result obtained by the simulation method no. 1

By Momentum simulation with 60 mesh, the input and output matching networks are designed to match the impedances obtained in the 1-tone characterization by the simulation method no. 1. Table 22 summarizes the dimensions of the components in the input and output matching network circuits designed based on the 1-tone characterization result obtained by the source & load pull simulation with method no. 1.

Table 22 : The dimensions of the components in the input and output matching network circuits designed based on the 1-tone characterization result obtained by the simulation method no. 1

	Dimension	TL1	TL2	TL3	TL4	TL5	TL6	Tee1	Tee2	Tee3
Input matching network	**Length (mil)**	312.30	183.80	279.00	287.50	108.30	549.20	90.17	90.17	90.17
	Width (mil)	90.17	90.17	90.17	90.17	90.17	90.17	90.17	90.17	90.17
Output matching network	**Length (mil)**	16.00	183.80	427.00	287.50	458.30	402.00	90.17	90.17	90.17
	Width (mil)	90.17	90.17	90.17	90.17	90.17	90.17	90.17	90.17	90.17

Figure 81 shows the layout of the input and output impedance matching network circuits designed for matching the impedances in the 1-characterizatio results obtained by the simulation method no. 1.

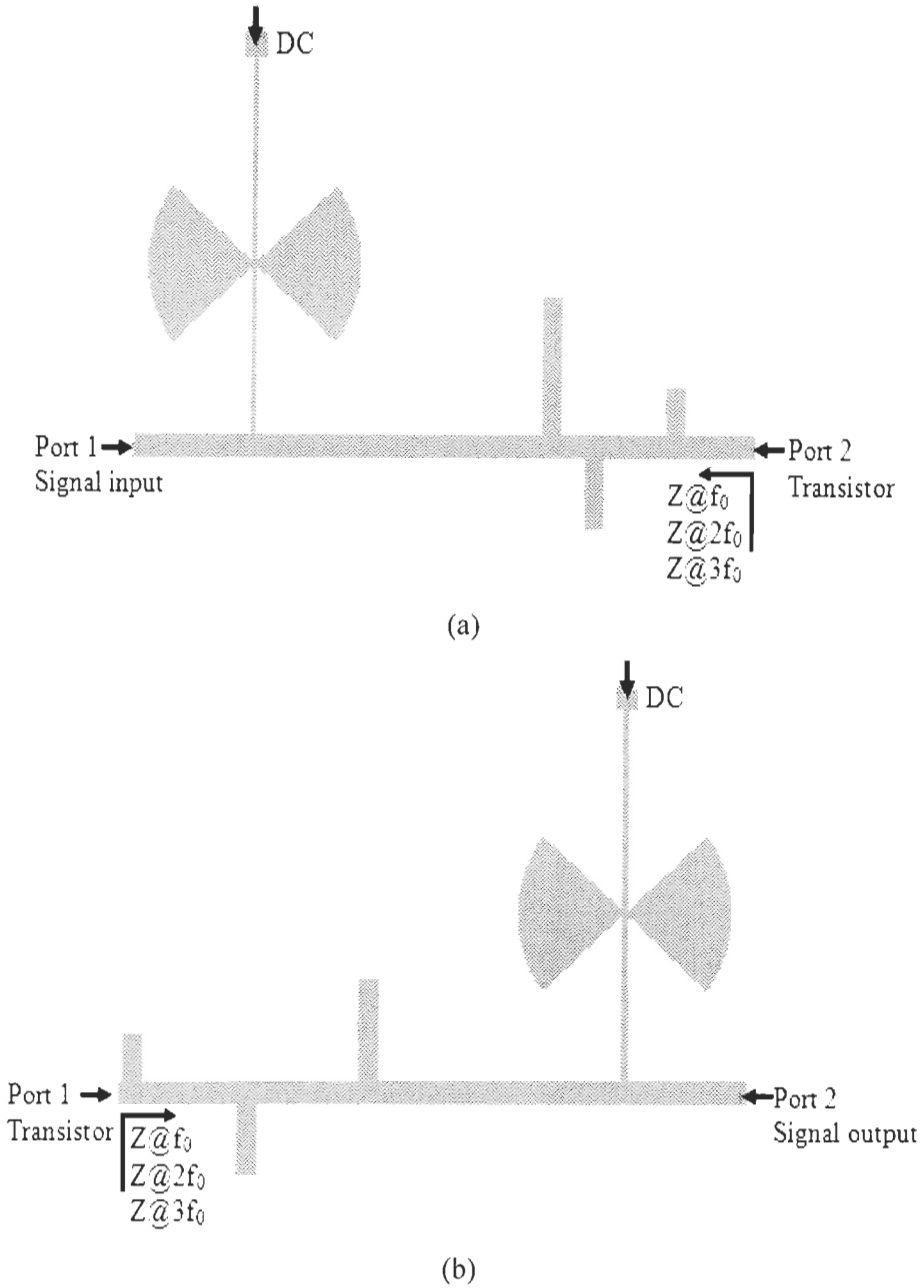


Figure 81 : Layout of the input (a) and output (b) matching network circuits designed based on the 1-tone characterization result obtained by the simulation method no. 1

Figure 82 and Figure 83 show the Momentum simulation results (60 mesh) of the input and output impedance matching network circuits for the 1-tone characterization result

obtained by the simulation method no. 1. The source and load impedances of the input and output matching network at 3.5 GHz, 7 GHz and 10.5 GHz simulated by Momentum simulation are compared with the target impedances in Table 23. Form Table 23, we can see that the input and output matching network are well designed to match the target impedances.

Table 23 : Impedances chosen in the 1-tone characterization by the simulation method no. 1 and the simulated impedances of the matching networks by Momentum simulation

	1-tone characterization result obtained by simulation (method no. 1)	**Momentum simulation results of the designed impedance matching networks**
Load imp. @ 3.5 GHz	0.566∠161.7°	0.571∠161.4°
Load imp. @ 7 GHz	1.000∠-178.0°	0.981∠-178.3°
Load imp. @ 10.5GHz	1.000∠132.0°	0.940∠132.1°
Source imp. @ 3.5 GHz	0.941∠-151.8°	0.941∠-151.9°
Source imp. @ 7 GHz	1.000∠28.0°	0.979∠27.7°
Source imp. @ 10.5GHz	1.000∠-135.0°	0.928∠-135.9°

The simulated insertion loss of the input matching network at 3.5 GHz is 1.03 dB. The suppression at 7 GHz and 10.5 GHz are 58.31 dB and 28.91 dB, respectively. The simulated insertion loss of the output matching network at 3.5 GHz is 0.12 dB. The suppression at 7 GHz and 10.5 GHz are 33.19 dB and 24.29 dB, respectively.

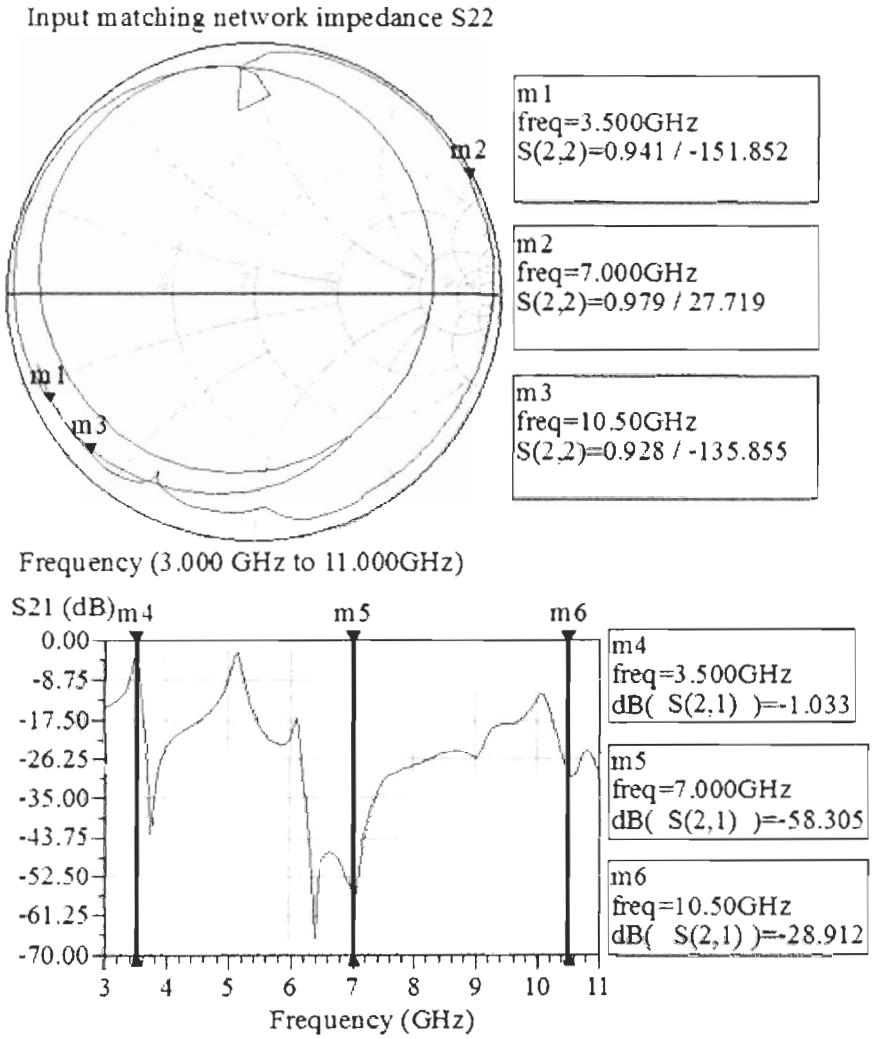


Figure 82 : Momentum simulation result of the input matching network designed based on the 1-tone characterization result obtained by the simulation method no. 1

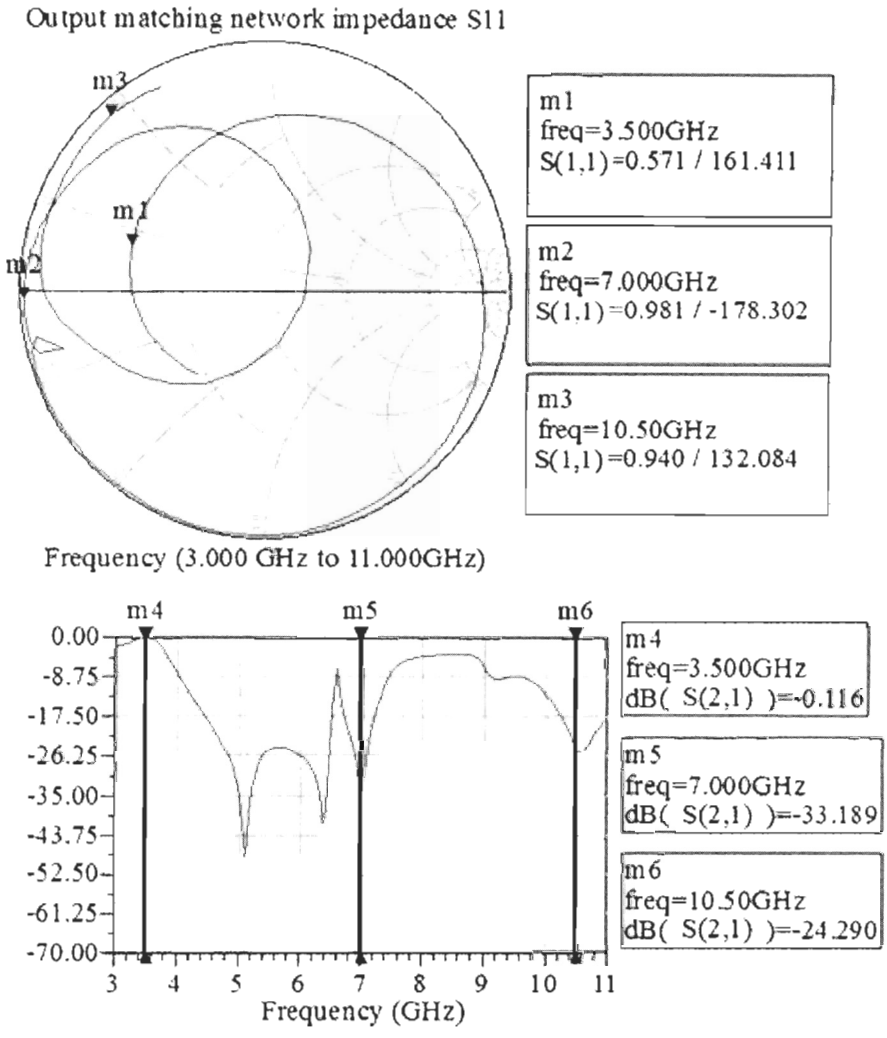


Figure 83 : Momentum simulation result of the output matching network designed based on the 1-tone characterization result obtained by the simulation method no. 1

5.4.2 Design of the matching network for the 1-tone characterization result obtained by the simulation method no. 2

The input and output matching network circuits are designed by Momentum simulation with 60 mesh to matching the impedances obtained in the characterization by the source & load pull simulation with method no. 2.

Table 24 summarizes the dimensions of the transmission lines in the input and output matching network circuits designed based on the 1-tone characterization result obtained by the source & load pull simulation with method no. 2.

Table 24 : The dimensions of the components in the input and output matching network circuits designed based on the 1-tone characterization result obtained by the simulation method no. 2

	Dimension	TL1	TL2	TL3	TL4	TL5	TL6	Tee1	Tee2	Tee3
Input matching network	**Length (mil)**	360.80	183.80	266.60	287.50	85.80	549.50	90.17	90.17	90.17
	Width (mil)	90.17	90.17	90.17	90.17	90.17	90.17	90.17	90.17	90.17
Output matching network	**Length (mil)**	351.80	183.80	623.50	287.50	139.50	385.00	90.17	90.17	90.17
	Width (mil)	90.17	90.17	90.17	90.17	90.17	90.17	90.17	90.17	90.17

Figure 84 shows the layout of the input and output impedance matching network circuits designed for matching the impedances in the 1-characterizatio results obtained by the simulation method no. 2.

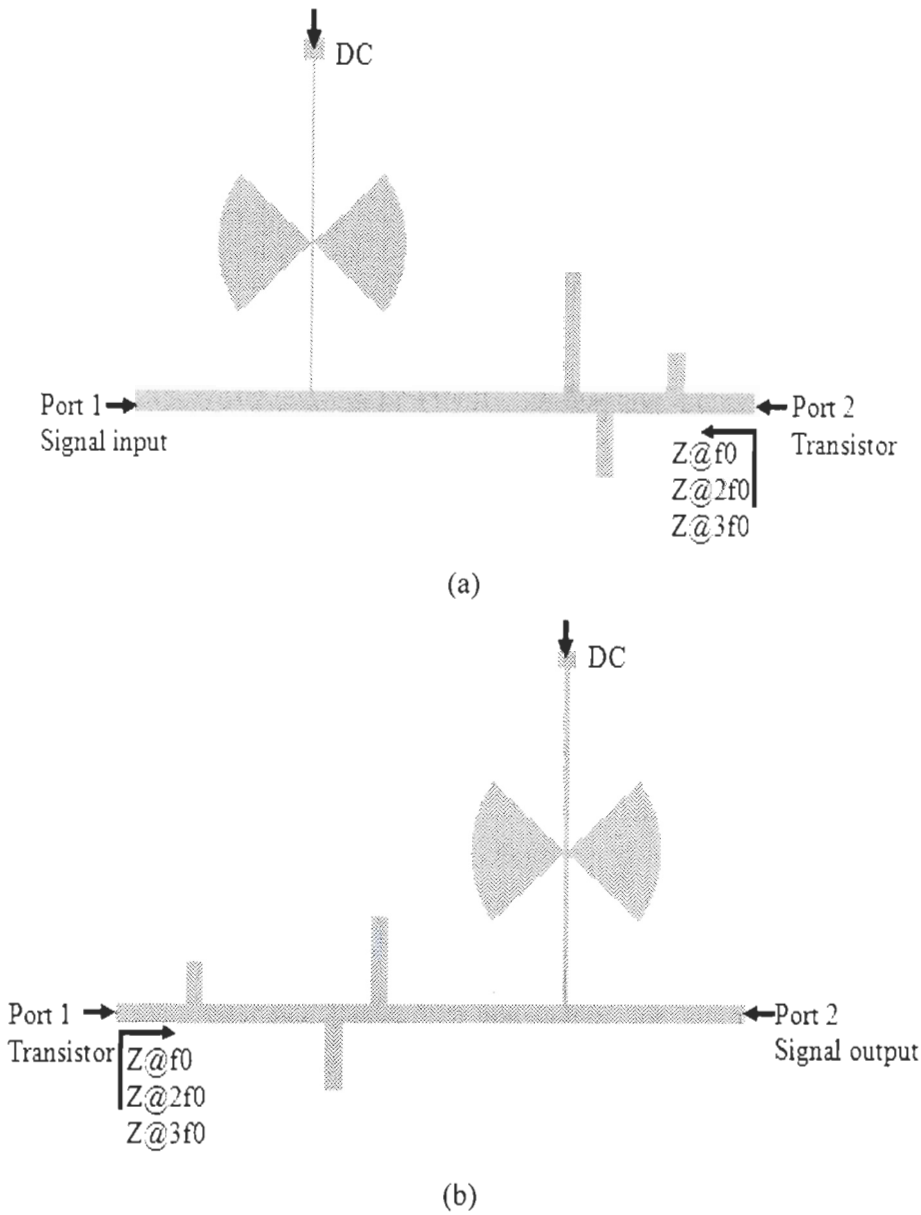


Figure 84 : Layout of the input (a) and output (b) matching network circuits designed based on the 1-tone characterization result obtained by the simulation method no. 2

Figure 85 and Figure 86 show the Momentum simulation results of the input and output impedance matching network circuits for the 1-tone characterization result obtained by the simulation method no. 2. The source and load impedances of the input and output matching network at 3.5 GHz, 7 GHz and 10.5 GHz simulated by Momentum simulation

with 60 mesh are compared with the target impedances in Table 25. Form Table 25, we can see that the input and output matching network are well designed to match the target impedances.

Table 25 : Impedances chosen in the 1-tone characterization by the simulation method no. 2 and the simulated impedances of the matching networks by Momentum simulation

	1-tone characterization results obtained by simulation (method no. 2)	**Momentum simulation results of the designed impedance matching networks**
Load imp. @ 3.5 GHz	0.705∠160.9°	0.706∠161.0°
Load imp. @ 7 GHz	1.000∠144.0°	0.934∠144.0°
Load imp. @ 10.5GHz	1.000∠-172.0°	0.935∠-172.1°
Source imp. @ 3.5 GHz	0.941∠-151.8°	0.940∠-151.3°
Source imp. @ 7 GHz	1.000∠0.0°	0.971∠0.6°
Source imp. @ 10.5GHz	1.000∠180.0°	0.931∠-179.8°

For the input impedance matching network designed based on the 1-tone characterization result obtained by the simulation method no. 2, the insertion loss at 3.5 GHz is 1.10 dB. The suppression at 7 GHz and 10.5 GHz are 58.51 dB and 27.57 dB, respectively.

For the output impedance matching network designed based on the 1-tone characterization result obtained by the simulation method no. 2, the insertion loss at 3.5 GHz is 0.10 dB. The suppression at 7 GHz and 10.5 GHz are 34.16 dB and 20.46 dB, respectively.

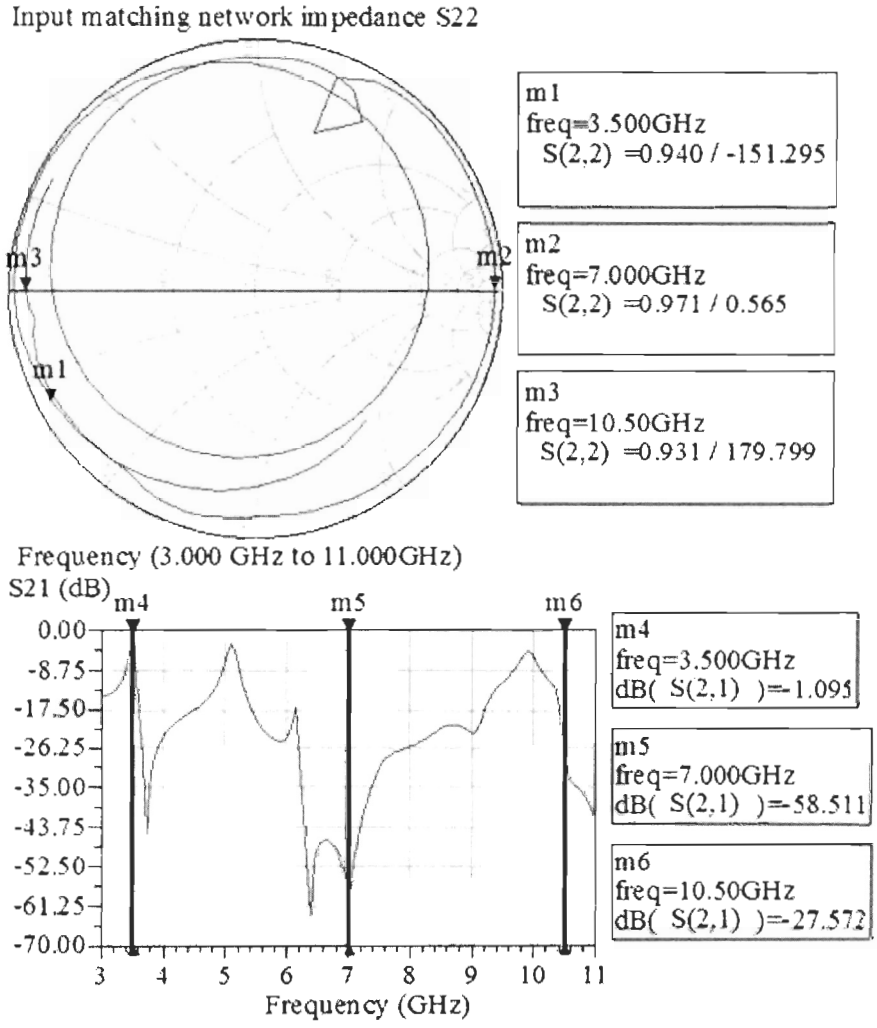


Figure 85 : Momentum simulation results of the input matching network based on the 1-tone characterization by the simulation method no. 2

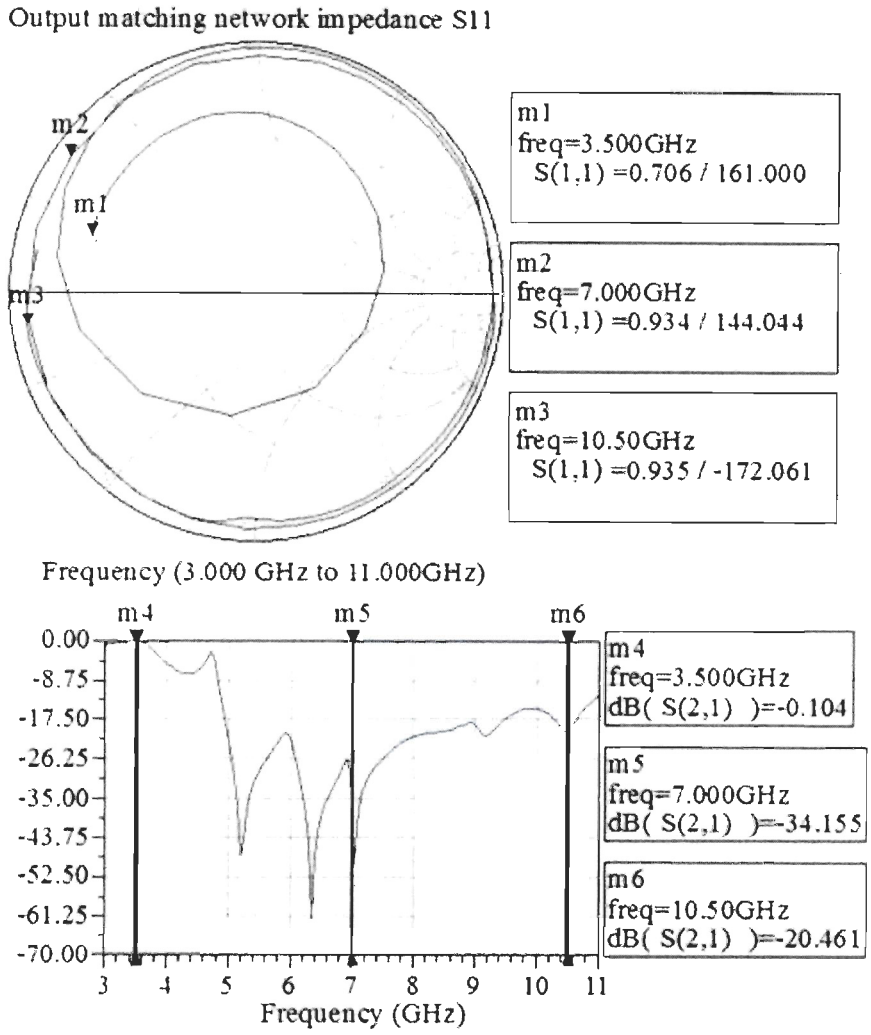


Figure 86 : Momentum simulation results of the output matching network based on the 1-tone characterization by the simulation method no. 2

5.4.3 Design of the matching network for the 1-tone characterization result obtained by the multi-harmonic tuner system

The input and output matching network circuits are designed by Momentum simulation with 60 mesh to matching the impedances obtained in the 1-tone

characterization results obtained by the multi-harmonic source & load pull tuner system from Focus microwaves Inc. Table 26 summarizes the dimensions of the components in the input and output matching network circuits designed based on the 1-tone characterization result obtained by the multi-harmonic source & load pull tuner system.

Table 26 : The dimensions of the components in the input matching network circuits designed based on the 1-tone characterization result obtained by the tuner system

	Dimension	TL1	TL2	TL3	TL4	TL5	TL6	Tee1	Tee2	Tee3
Input matching network	**Length (mil)**	239.30	183.20	573.60	287.50	32.50	490.00	90.17	90.17	90.17
	Width (mil)	90.17	90.17	90.17	90.17	90.17	90.17	90.17	90.17	90.17
Output matching network	**Length (mil)**	115.00	183.80	286.10	287.50	475.10	371.00	90.17	90.17	90.17
	Width (mil)	90.17	90.17	90.17	90.17	90.17	90.17	90.17	90.17	90.17

Figure 87 shows the layout of the input and output impedance matching network circuits designed for matching the source and load impedances in the 1-tone characterization by the multi-harmonic source & load pull tuner system from Focus microwaves Inc.

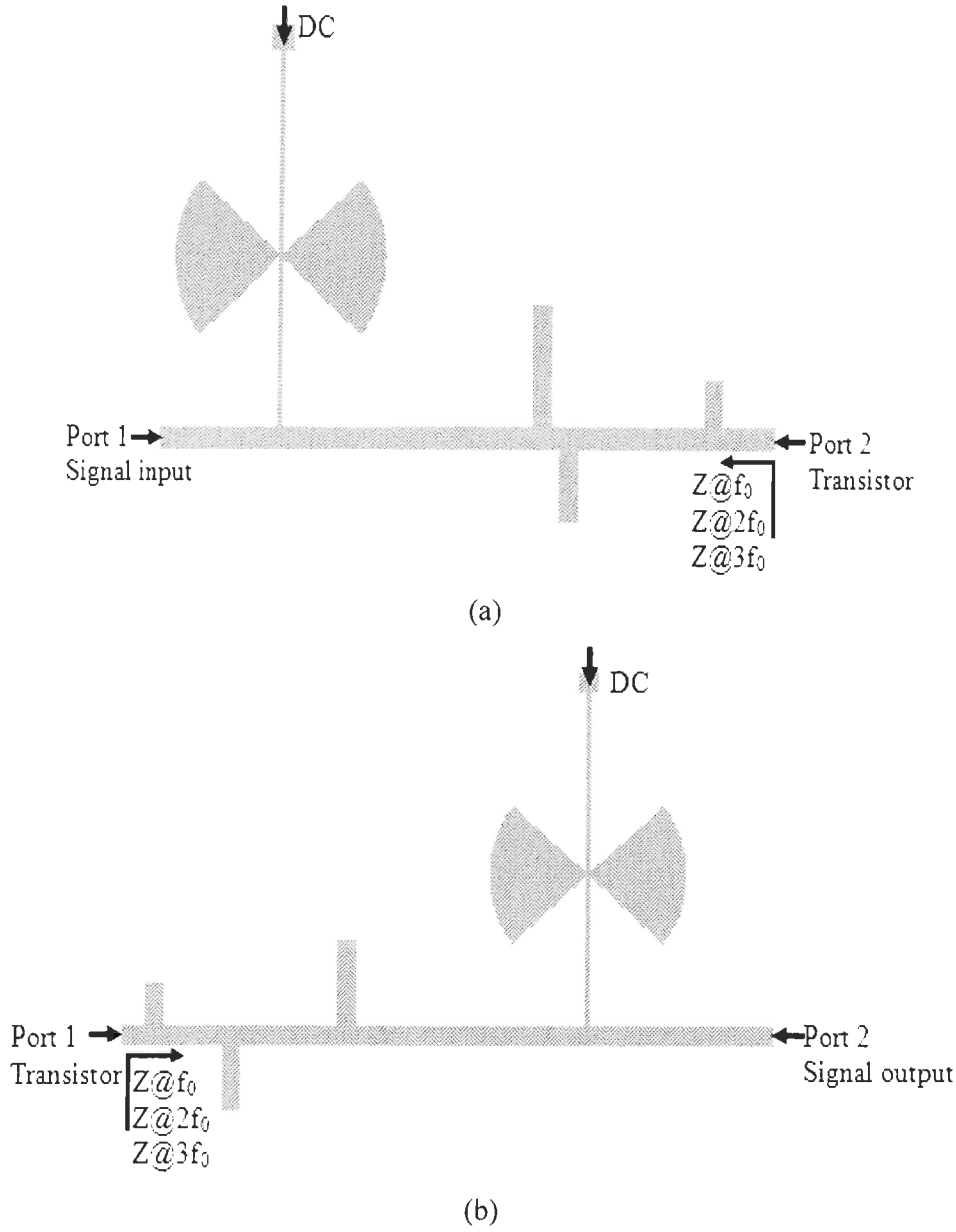


Figure 87 : Layout of the input (a) and output (b) matching network circuits designed based on the 1-tone characterization result obtained by the tuner system

Figure 88 and Figure 89 show the Momentum simulation results of the input and output impedance matching network circuits for matching the source and load impedances in the 1-tone characterization by the multi-harmonic source & load pull tuner system.

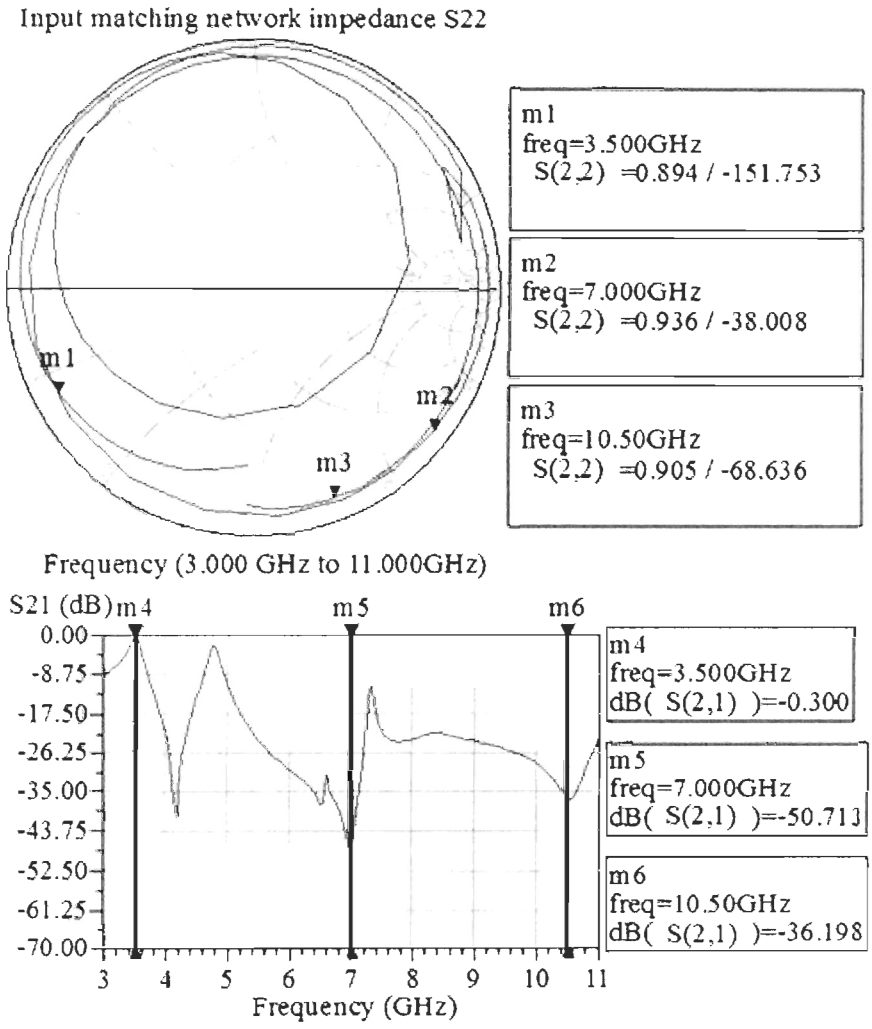


Figure 88 : Momentum simulation results of the input matching network designed based on the 1-tone characterization by the tuner system

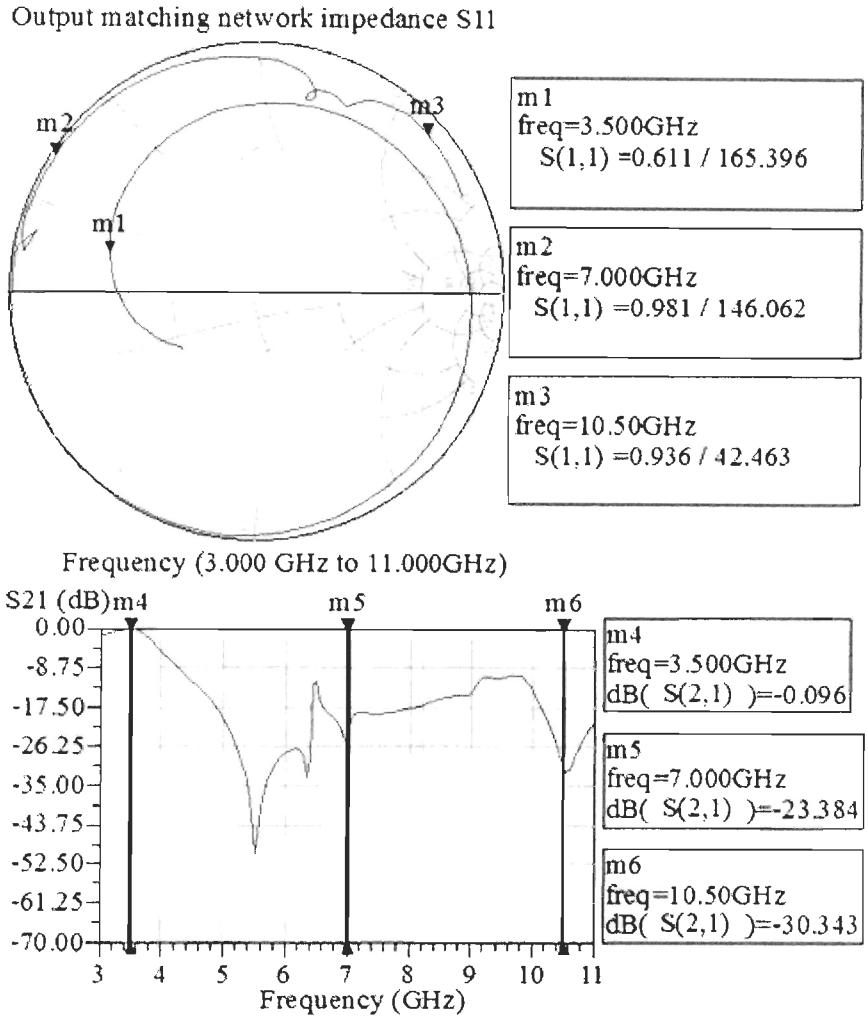


Figure 89 : Momentum simulation results of the output matching network designed based on the 1-tone characterization by the tuner system

The source and load impedances of the input and output matching network at 3.5 GHz, 7 GHz and 10.5 GHz simulated by Momentum simulation with 60 mesh are compared with the target impedances in Table 27. From this table, we can see that the input and output matching network are well designed to match the target impedances.

Table 27 : Impedances chosen in the 1-tone characterization by the tuner system and the simulated impedances of matching networks by Momentum simulation

	1-tone characterization results obtained by the source & load pull tuner system	**Momentum simulation results of the designed impedance matching networks**
Load imp. @ 3.5 GHz	0.603∠165.5°	0.611∠165.4°
Load imp. @ 7 GHz	0.938∠146.1°	0.981∠146.1°
Load imp. @ 10.5GHz	0.918∠42.6°	0.936∠42.5°
Source imp. @ 3.5 GHz	0.892∠-151.7°	0.894∠-151.8°
Source imp. @ 7 GHz	0.900∠-38.5°	0.936∠-38.0°
Source imp. @ 10.5GHz	0.880∠-68.6°	0.905∠-68.6°

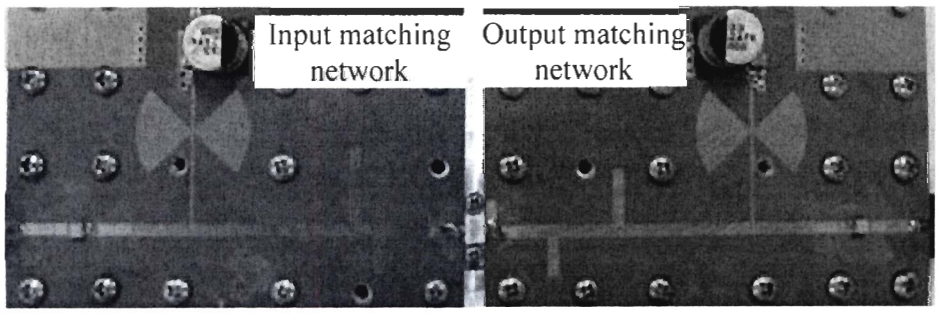
For the input impedance matching network designed based on the 1-tone characterization result obtained by the multi-harmonic source & load pull tuner, the simulated insertion loss at 3.5 GHz is 0.30 dB. The suppression at 7 GHz and 10.5 GHz are 50.71 dB and 36.20 dB, respectively.

For the output impedance matching network designed based on the 1-tone characterization result obtained by the multi-harmonic source & load pull tuner, the simulated insertion loss at 3.5 GHz is 0.10 dB. The suppression at 7 GHz and 10.5 GHz are 23.38 dB and 30.34 dB, respectively.

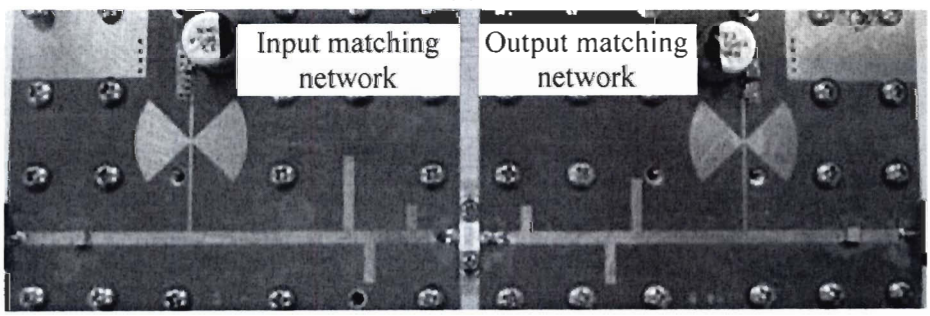
5.5 EVALUATIONS OF THE 1-TONE CHARACTERIZATION RESULTS

To evaluate the 1-tone characterization results obtained by the multi-harmonic tuner system and by the simulation in chapter 2, the 1-tone inverse class F PA circuits are fabricated. Rogers RT/duroid 5870 with 31 mil substrate thickness and 35 μm metal

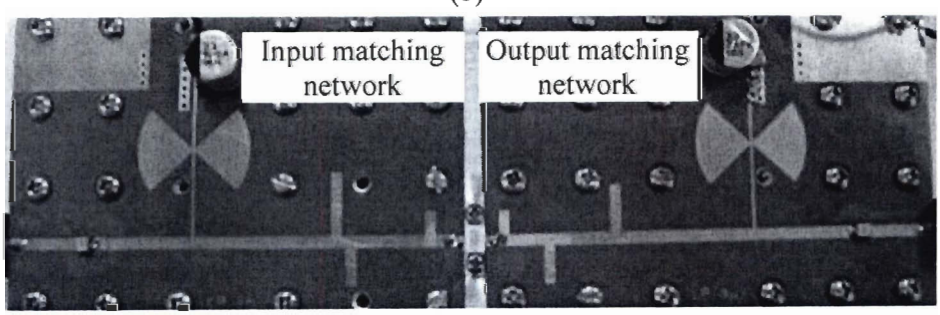
thickness is used. The fabricated 1-tone inverse class F PAs designed based on the characterization result obtained by the simulation method no. 1 and no. 2 are shown in Figure 90 (a) and (b). The fabricated 1-tone inverse class F PA designed based on the characterization result obtained by the tuner system is shown in Figure 90 (c). For each PA circuits, ATC 100B capacitor of 51 pF capacitance is used as the blocking capacitor. Panasonic's 33 μF aluminum capacitor is used in the bias circuit as the bypass capacitor.



(a)



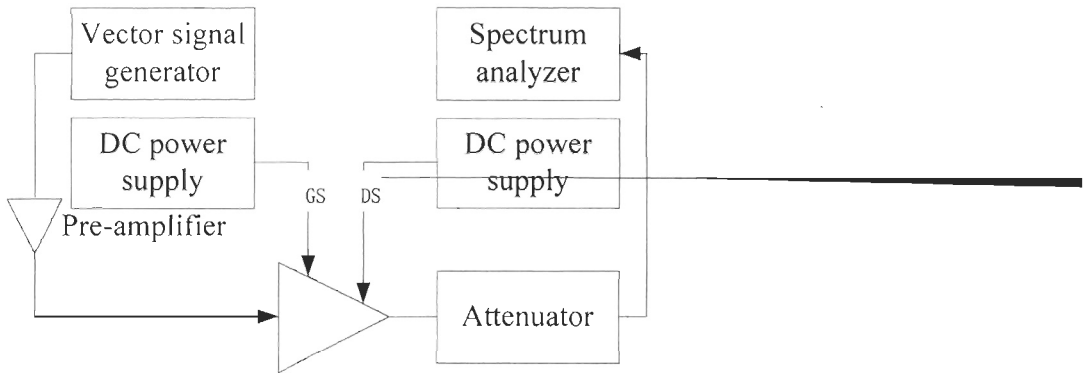
(b)



(c)

Figure 90 : Fabricated PA designed based on the 1-tone characterization by the simulation method no. 1 (a), method no. 2 (b) and by the source & load pull tuner system (c)

For measuring the fabricated inverse class F PAs, the setup shown in Figure 91 is used. Rohde & Schwarz SMBV100A vector signal generator is used to generate the 1-tone signal. N6705B DC power analyzer is used to provide DC power. Agilent MXA signal analyzer is used to measure the signal. ZHL 4240 amplifier from Mini Circuits Inc. is used as a pre-amplifier. Aeroflex Weinschel 40-30-34 attenuator is added on the right side of the fabricated inverse class F PA. The measured attenuation of this attenuator at 3.5 GHz is 31.7 dB.



Fabricated inverse class F PA

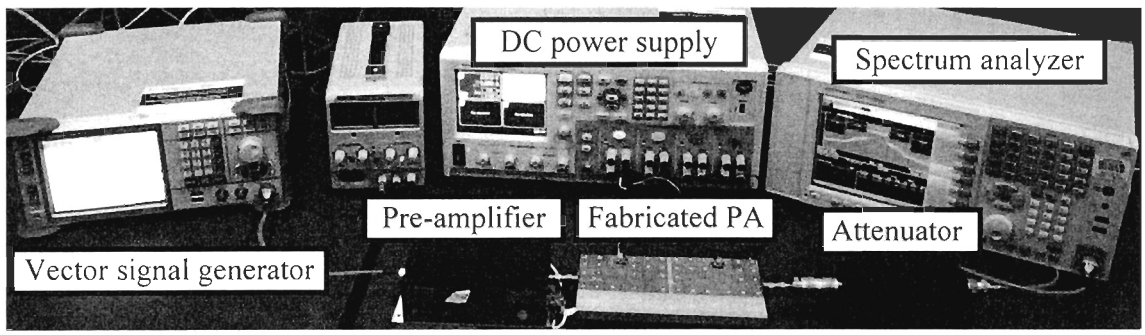
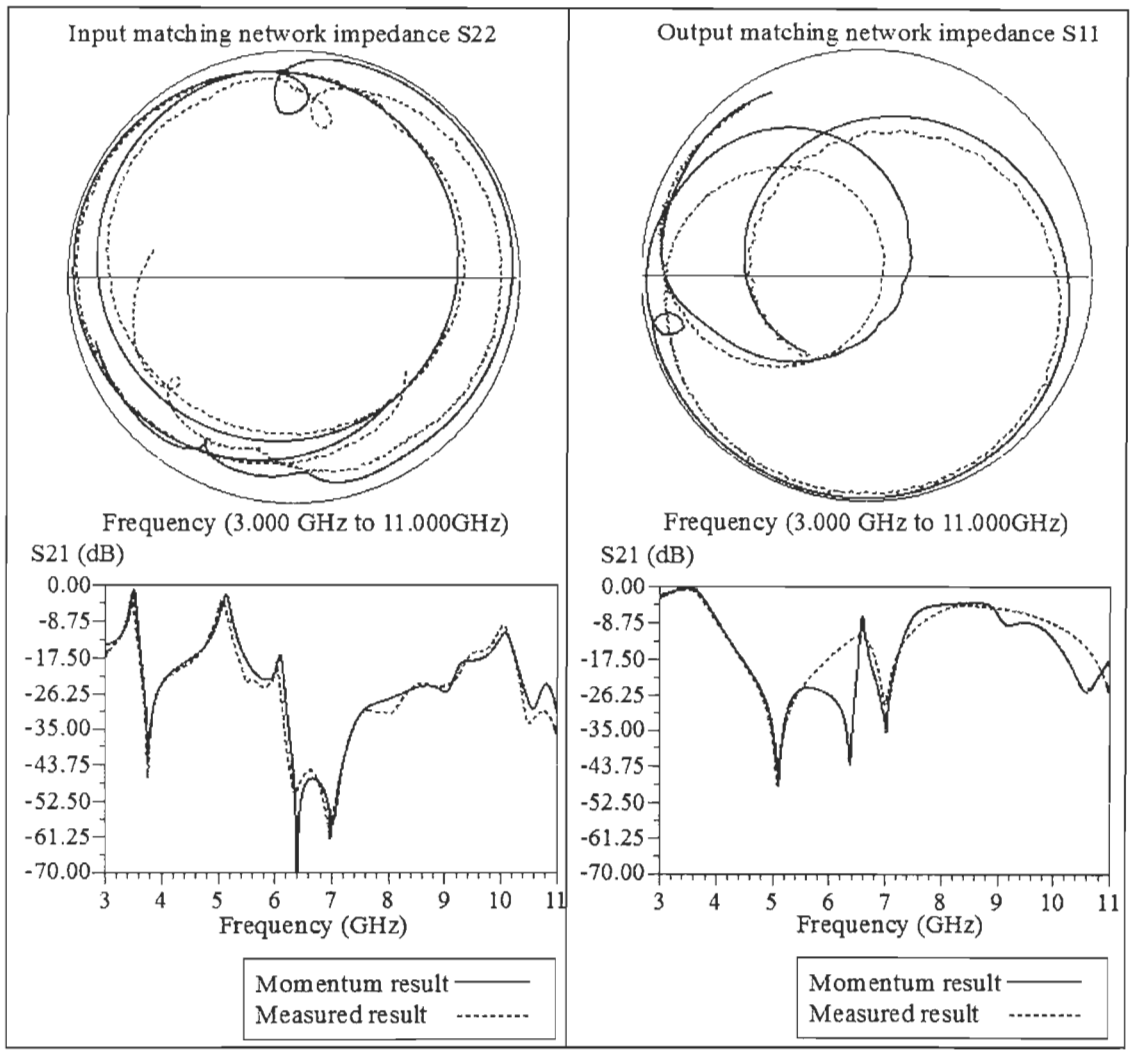


Figure 91 : Setup for measuring the fabricated inverse class F PA

5.5.1 Evaluation of the 1-tone characterization results obtained by the simulation with method no. 1

In this part, the 1-tone inverse class F PA designed based on the 1-tone characterization by the simulation method no. 1 is fabricated. It is measured to evaluate the

results obtained in characterization. The measured impedances and insertion loss of the input and output matching network of this PA are compared with the Momentum simulation results in Figure 92.



(a) (b)

Figure 92 : Comparison of the measured and simulated impedances and insertion loss of the input (a) and output (b) matching networks designed based on the 1-tone characterization by the simulation method no. 1

The measured impedances and S_{21} of the matching network circuits are compared with the simulation results in Table 28. By comparison, we can see that the tendencies of the measured impedances and the insertion loss of matching network are similar to the simulation results. There are 6.6°, 6.7° and 3.6° phase differences between the measured and simulated phase of the load impedance at 3.5 GHz, 7 GHz and 10.5 GHz, respectively. On the other hand, there are 1.0°, 4.6° and 27.3° phase differences between the measured and simulated phase of the source impedance at 3.5 GHz, 7 GHz and 10.5 GHz, respectively. In the output matching network, the measured suppression at 10.5 GHz is only 13.46 dB while the simulated suppression at 10.5 GHz is 24.29 dB. The measured frequency suppressed by the 3rd harmonic control circuit of the matching network is shifted from 10.5 GHz to 11 GHz after the fabrication. These errors may be caused by my design method or fabrication.

Table 28 : The measured and simulated results of impedances and S_{21} of matching network circuits designed based on the 1-tone characterization by the simulation method no. 1

	Measured impedances of matching networks	**Simulated impedances of matching networks by Momentum simulation**	**Measured S_{21} (dB)**	**Simulated S_{21} by Momentum simulation (dB)**
Load imp. @ 3.5 GHz	0.546∠154.5°	0.571∠161.4°	-0.44	-0.12
Load imp. @ 7 GHz	0.890∠175.0°	0.981∠-178.3°	-28.55	-33.19
Load imp. @ 10.5GHz	0.938∠135.7°	0.940∠132.1°	-13.46	-24.29
Source imp. @ 3.5 GHz	0.941∠-152.9°	0.941∠-151.9°	-2.08	-1.03
Source imp. @ 7 GHz	0.921∠23.1°	0.979∠27.7°	-58.32	-58.31
Source imp. @ 10.5GHz	0.746∠-163.2°	0.928∠-135.9°	-33.88	-28.91

When this fabricated inverse class F PA is biased at V_{GS}=-2.58 V and V_{DS}=28 V, the PAE and gain are measured. The measured and simulated results of this inverse class F PA are shown in Figure 93.

With a 1-tone signal at 3.5 GHz, the measured maximum PAE 69.58% is found when input power is 28.59 dBm with 40.41 dBm output power. When the input power is 25 dBm, the output power is 39.42 dBm, the measured PAE is 65.56%. In chapter 2, the 1-tone characterization result by ADS simulation with method no. 1 shows that a 77.00% PAE and a 41.13 dBm output power can be obtained when the input power is 25 dBm. There is 11.44% difference in PAE and 1.71 dBm difference in output power. Based on Table 1, if the 3rd harmonic is not well controlled, the efficiency could be decreased to 67%. Therefore, we assume that the difference between the measured PAE and output power and the simulation results is caused by that the load 3rd harmonic is not well suppressed by the output matching network, or the model of the transistor is not precise enough.

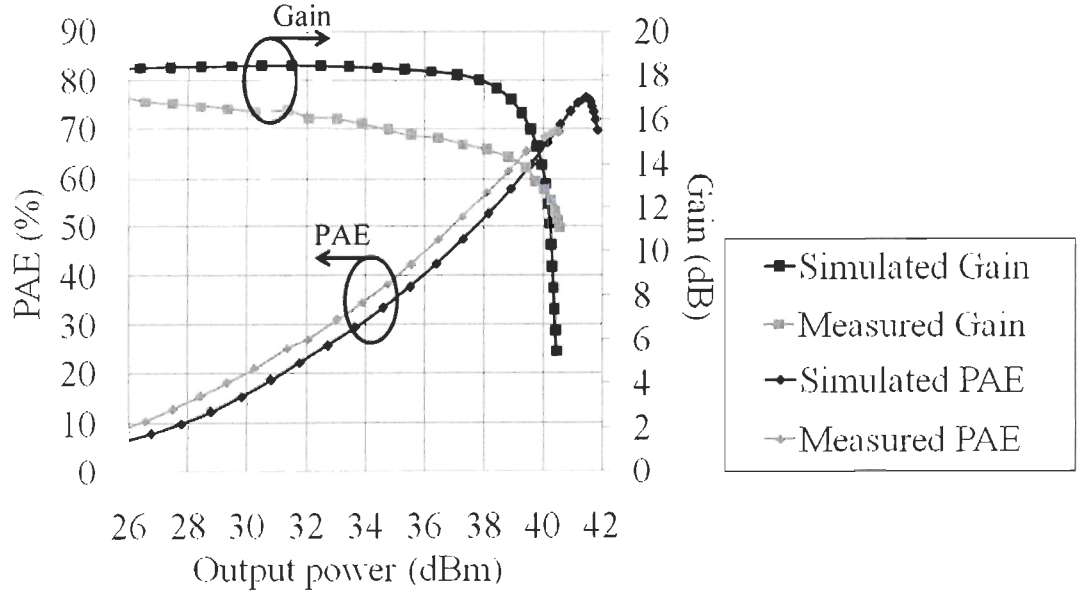


Figure 93 : Measured (grey) and simulated (black) PAE and gain versus the output power for 1-tone inverse class F PA designed based on the characterization by the simulation method no. 1

Figure 94 shows the measured and simulated maximum PAE, output power and gain across a frequency range from 3.4 GHz to 3.6 GHz. In the frequency band 3.45-3.55 GHz, the measured PAE is between 27.63% and 69.58%, and measured output power is between

34.90 dBm and 40.41 dBm. Compared with the simulation results, measured PAE, output power and gain of fabricated inverse class F PA are lower. In the frequency band 3.45-3.55 GHz, there are 6.86-33.41% difference in PAE and 0.24-5.03 dB difference in gain.

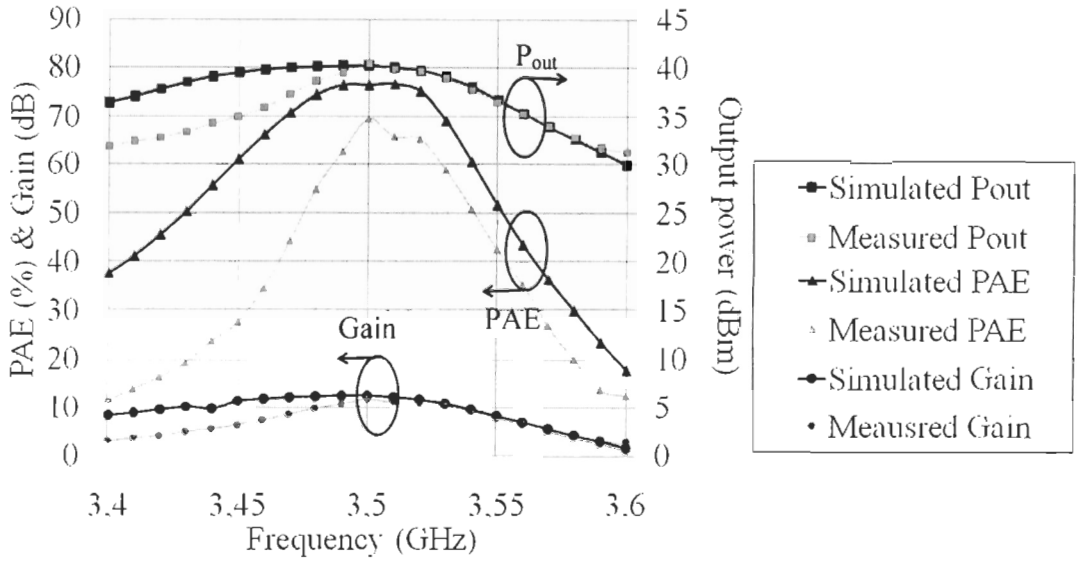
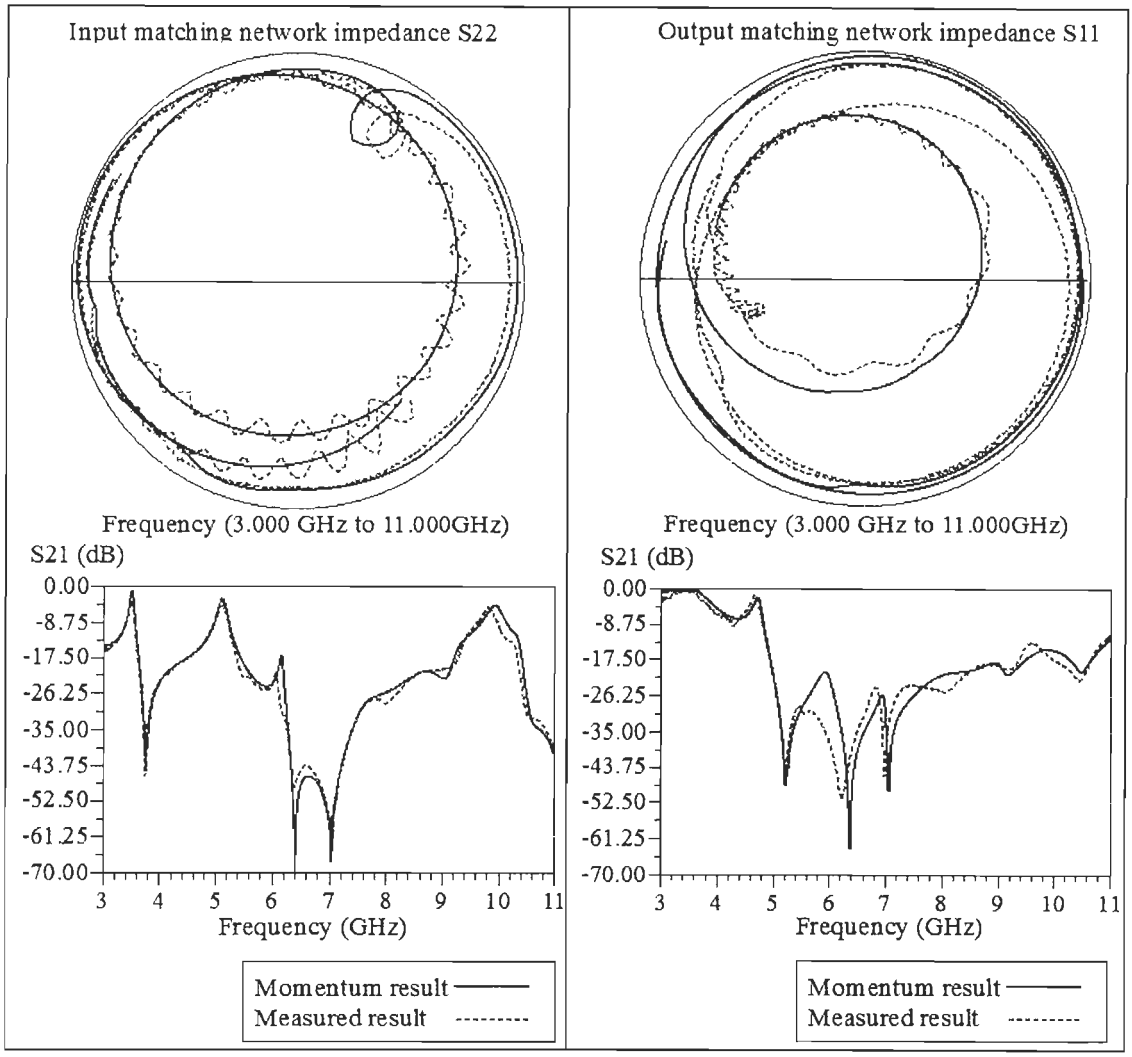


Figure 94 : Measured (gray) and simulated (black) PAE, output power and gain of inverse class F PA designed based on the characterization by ADS simulation with method no. 1 across a frequency range from 3.4 GHz to 3.6 GHz

5.5.2 Evaluation of the 1-tone characterization results obtained by the simulation with method no. 2

In this part, the 1-tone inverses class F PA designed based on the 1-tone characterization by the simulation method no. 2 is measured to evaluate the results obtained in characterization. The measured impedances and insertion loss of the input and output matching network for the 1-tone inverse class F PA designed based on the characterization by the simulation method no. 2 are compared with the Momentum simulation results in Figure 95.



(a) (b)

Figure 95 : Comparison of measured and simulated impedances and insertion loss of the input (a) and output (b) matching networks designed based on the 1-tone characterization by the simulation method no. 2

The measured impedances and S_{21} of the matching network circuits are compared with the simulation results obtained by Momentum simulation with 60 mesh in Table 29. By comparison, we can see that the tendencies of the measured impedances and insertion loss of the input and output matching network are similar to the simulation results. The 2^{nd} and 3^{rd} harmonics are well suppressed by the input and output matching network. However,

there are 6.5°, 35.4° and 14.1° phase differences between the measured and simulated phase of the load impedance at 3.5 GHz, 7 GHz and 10.5 GHz. 0.8°, 10.0° and 4.2° phase differences are existed between the measured and simulated phase of the source impedance at 3.5 GHz, 7 GHz and 10.5 GHz. These errors may be caused by my design method or fabrication.

Table 29 : The measured and simulated results of impedances and S_{21} of matching network circuits designed based on the 1-tone characterization by the simulation method no. 2

	Measured impedances of matching networks	**Simulated impedances of matching networks by Momentum simulation**	**Measured S_{21} (dB)**	**Simulated S_{21} by Momentum simulation (dB)**
Load imp. @ 3.5 GHz	0.714∠154.5°	0.706∠161.0°	-0.48	-0.10
Load imp. @ 7 GHz	0.730∠108.6°	0.934∠144.0°	-40.63	-34.16
Load imp. @ 10.5GHz	0.772∠173.8°	0.935∠-172.1°	-21.82	-20.46
Source imp. @ 3.5 GHz	0.939∠-152.1°	0.940∠-151.3°	-1.97	-1.10
Source imp. @ 7 GHz	0.935∠-10.6°	0.971∠0.6°	-57.82	-58.51
Source imp. @ 10.5GHz	0.939∠175.6°	0.931∠179.8°	-31.49	-27.57

When this fabricated inverse class F PA is biased at V_{GS}=-2.58 V and V_{DS}=28 V, the PAE and gain of the 1-tone inverse class F PA designed based on the characterization by the simulation method no. 2 are measured with a 1-tone signal at 3.5 GHz. The measured and simulated results of this inverse class F PA are shown in Figure 96. When input power is 25 dBm, the PAE reaches maximum value 69.98% with 38.62 dBm output power. In chapter 2, the 1-tone characterization result by the simulation method no. 2 shows 78.29% PAE and 40.12 dBm output power with 25 dBm input power. There is 8.31% difference in PAE and 1.50 dBm difference in output power. We assume that because the impedances achieved by the matching network are shifted after fabrication, the measured PAE and

output power are different from the designed impedances in Momentum simulation. These differences can also be caused by the imprecise model of the transistor.

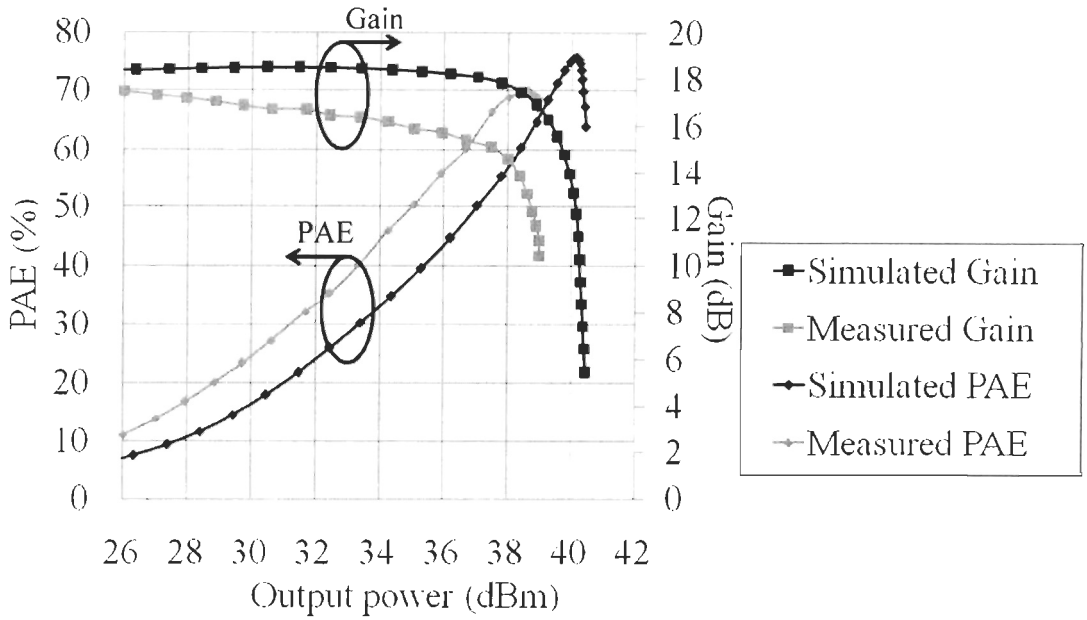


Figure 96 : Measured (grey) and simulated (black) PAE and gain versus output power for the 1-tone inverse class F PA based on the characterization by the simulation method no. 2

Figure 97 shows the measured maximum PAE, output power and gain across a frequency range from 3.4 GHz and 3.6 GHz. The measured maximum PAE is found at 3.49 GHz with 38.80 dBm output power. In the frequency band 3.45-3.55 GHz, the measured PAE is between 41.08% and 71.48%, and the measured output power is between 35.23 dBm and 38.80 dBm. Compared with the simulation results, the measured PAE, output power and gain of fabricated inverse class F PA are lower. In the frequency band 3.45-3.55 GHz, there is 2.15-23.56% and 0.10-1.07 dB difference in PAE and gain, respectively,.

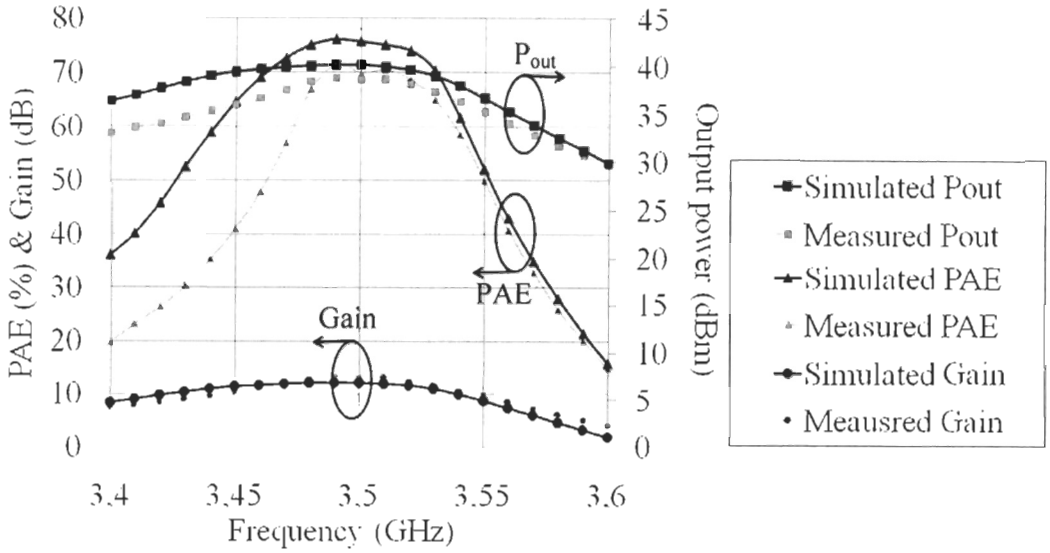
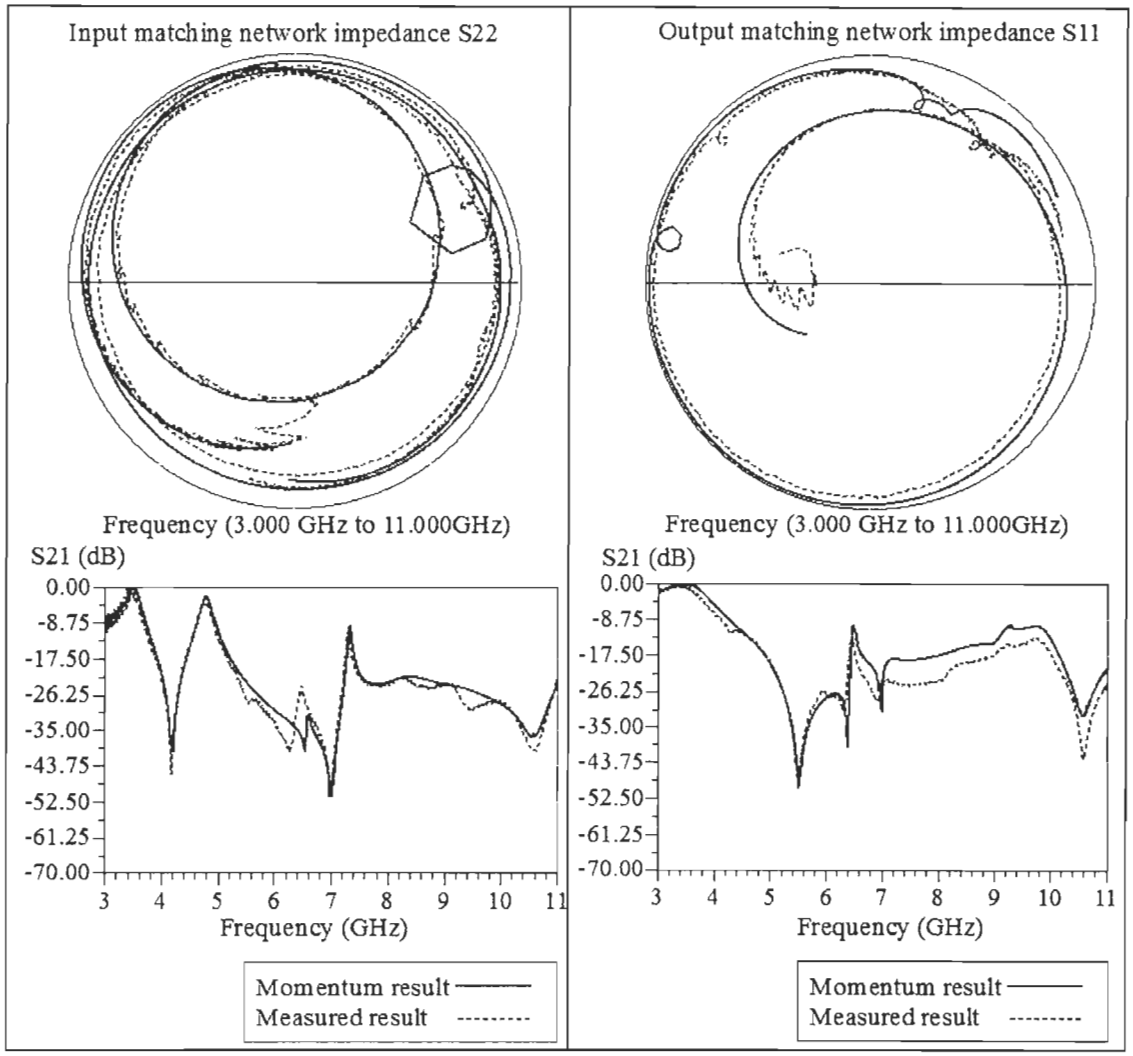


Figure 97 : Measured (grey) and simulated (black) PAE, output power and gain versus output power for the 1-tone inverse class F PA based on the characterization by the simulation method no. 2 across bandwidth of 3.4 GHz to 3.6 GHz

5.5.3 Evaluation of the 1-tone characterization results obtained by the multi-harmonic tuner system

In this part, the 1-tone inverses class F PA designed based on the 1-tone characterization by the multi-harmonic tuner system is measured to evaluate the results obtained in characterization. The measured impedances and insertion loss of the input and output matching network designed based on the characterization results obtained by the multi-harmonic source & load pull tuner are compared with the Momentum simulation results in Figure 98.



(a) (b)

Figure 98 : Comparison of measured and simulated impedances and insertion loss of the input (a) and output (b) matching networks designed based on the 1-tone characterization by the tuner system

The measured impedances and S_{21} of the matching network circuits are compared with the simulation results obtained by Momentum simulation with 60 mesh in Table 30. By comparison, we can see that the tendencies of the measured impedances and insertion loss of input and output matching network are similar to the simulation results. The 2^{nd} and 3^{rd} harmonics are well suppressed by the input and output matching network. However,

there are 19.2°, 34.0° and 14.1° phase differences between the measured and simulated phase of the load impedance at 3.5 GHz, 7 GHz and 10.5 GHz. 3.9°, 15.2° and 11.4° phase differences are existed between the measured and simulated phase of the source impedance at 3.5 GHz, 7 GHz and 10.5 GHz. These errors may be caused by my design method or fabrication.

Table 30 : The measured and simulated results of impedances and S_{21} of matching network circuits designed based on the 1-tone characterization by the tuner system

	Measured impedances of matching networks	**Simulated impedances of matching networks by Momentum simulation**	**Measured S_{21} (dB)**	**Simulated S_{21} by Momentum simulation (dB)**
Load imp. @ 3.5 GHz	0.614∠146.2°	0.611∠165.4°	-1.05	-0.10
Load imp. @ 7 GHz	0.948∠112.2°	0.981∠146.1°	-28.61	-22.34
Load imp. @ 10.5GHz	0.886∠28.4°	0.936∠42.5°	-42.78	-31.82
Source imp. @ 3.5 GHz	0.881∠-155.7°	0.894∠-151.8°	-1.57	-0.46
Source imp. @ 7 GHz	0.867∠-53.2°	0.936∠-38.0°	-51.11	-50.71
Source imp. @ 10.5GHz	0.906∠-80.0°	0.905∠-68.6°	-38.72	-36.20

When this fabricated inverse class F PA is biased at V_{GS}=-2.58 V and V_{DS}=28 V, the PAE and gain of the 1-tone inverse class F PA designed based on the characterization results by the tuner system are measured with a 1-tone signal at 3.5 GHz as shown in Figure 99. When input power is 25 dBm, measured PAE is 75.80% with 39.20 dBm output power. In chapter 1, the 1-tone characterization result by the source & load pull tuner system shows 74.21% PAE and 39.92 dBm output power with 25 dBm input power. There are 1.59% difference in PAE and 0.72 dBm difference in output power. At 3.5 GHz, the measured maximum PAE of the PA 79.76% is found when the input power is 27.94 dBm with 40.02 dBm output power.

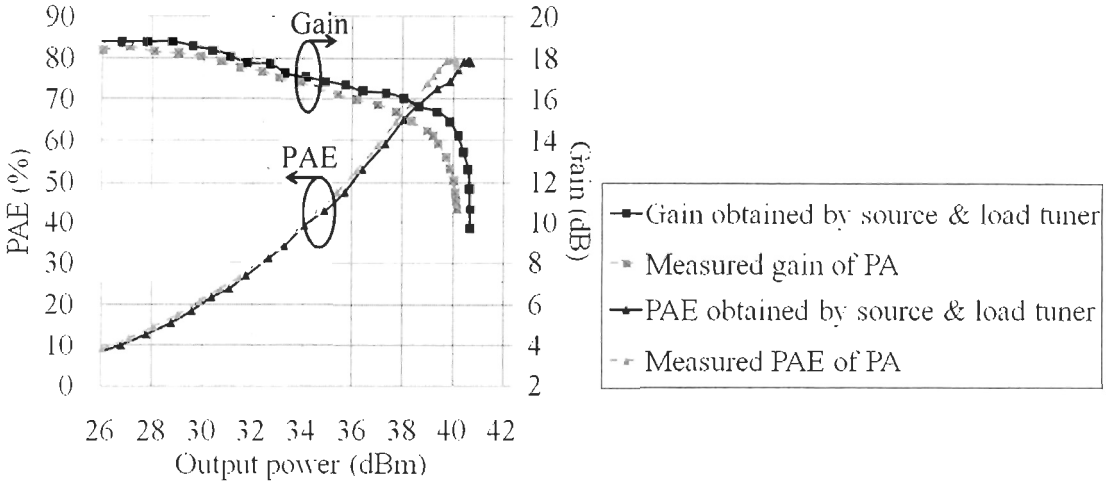


Figure 99 : Measured PAE and gain by tuner system (black) and measured PAE and gain of the 1-tone inverse class F PA designed based on the 1-tone characterization by the tuner system (gray)

Figure 100 shows the measured PAE and gain across a frequency range of 3.4 GHz and 3.6 GHz when the input power is 27.94 dBm. The measured maximum PAE 80.49% is found at 3.49 GHz with 40.32 dBm output power. In the frequency band 3.45-3.55 GHz, the measured PAE is between 51.33% and 80.49%, and the measured output power is between 40.40 dBm and 39.72 dBm.

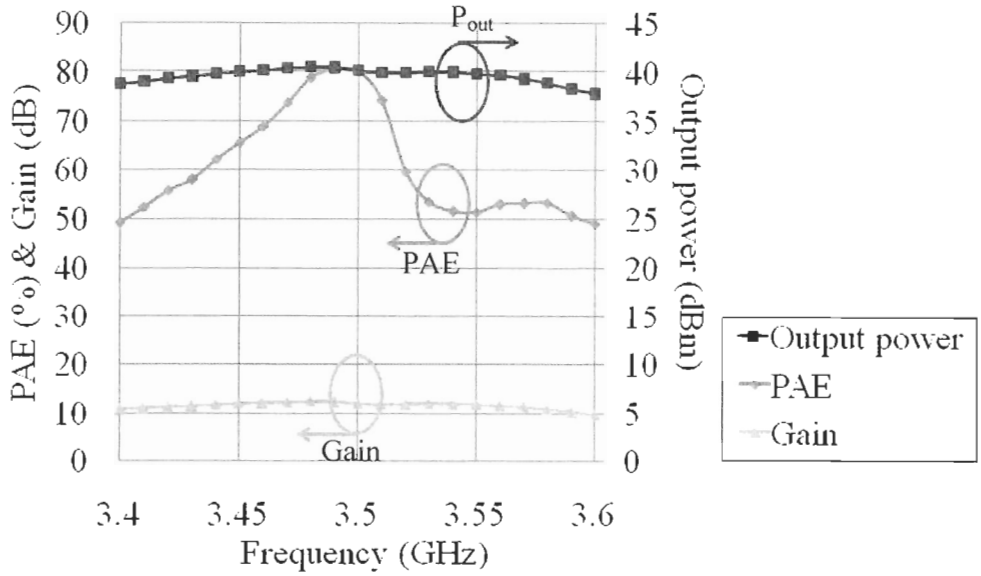


Figure 100 : Measured PAE, gain and output power of the 1-tone inverse class F PA designed based on the 1-tone characterization by the tuner system across a bandwidth of 3.4 GHz to 3.6 GHz

Table 31 summarizes the published work for the CGH40010 transistor. From this table, we can see that the PAE of the 1-tone inverse class F PA designed based on the 1-tone characterization by the tuner system is the highest when the output power is more than 40 dBm at 3.5 GHz.

Table 31 : Published works of PA with CGH40010 transistor

References	**Transistor**	**Frequency (GHz)**	**Max PAE (%)**	**P_{out} (dBm)**	**Gain (dB)**
(Jee *et al.*, 2012)	CGH40010	3.50	75.80	40.20	15.80
(Xu *et al.*, 2010)	CGH40010	3.50	70.01	39.93	11.93
(Moon *et al.*, 2012a)	CGH40010	2.66	73.50	41.00	12.00
(Moon *et al.*, 2010)	CGH40010	2.14	77.30	40.60	15.60
(Kim *et al.*, 2008)	CGH40010	1.00	74.10	39.58	13.76
(Kim *et al.*, 2009)	CGH40010	3.20	73.20	38.30	13.30
This work	CGH40010	3.50	79.76	40.02	12.08

5.5.4 Conclusion of the evaluations of the 1-tone characterization results

Based on the different characterization methods, the inverse class F PAs are designed with the same substrate (Rogers RT/duroid 5870 with 31 mil substrate thickness and 35 μm metal thickness), fabricated in the same facility (Poly-Grames research center) and measured in the same conditions. From the measured results, we notice that the measured results of the fabricated inverse class F PAs are not always similar to the results obtained in the characterizations. Table 32 summarizes the final results (PAE and output power) in characterizations and the measured results of the fabricated inverse class F PAs.

Table 32 : The final results in the 1-tone characterizations and the measured results of the fabricated inverse class F PAs

Characterization method	**Characterization results**		**Measured results of fabricated PAs**		**Difference between the characterization results and the measured results of fabricated PAs**	
	PAE (%)	**Pout (dBm)**	**PAE (%)**	**Pout (dBm)**	**PAE (%)**	**Pout (dBm)**
By simulation with method no. 1	77.00	41.13	65.56	39.42	11.44	1.71
By simulation with method no. 2	78.79	40.12	69.98	38.62	8.81	1.14
By source & load pull tuner	74.21	39.92	75.80	39.20	1.59	0.72

From Table 32, we can see that the multi-harmonic source & load pull tuner predicts the PAE and output power more precisely than the source & load pull simulation with large signal model. Thus, to achieve a first-pass design for an inverse class F PA, the multi-harmonic source & load pull tuner is recommended.

5.6 PROPOSED STRUCTURE OF THE MATCHING NETWORK FOR THE LTE INVERSE CLASS F PA

From the comparison between the Momentum simulation results and the measured results of the 1-tone matching networks, we can see that in some case, the suppressed frequencies are shifted after fabrication. Based on (Wang *et al.*, 2012b), by using the microstrip radial stub, wider bandwidth of harmonic suppression could be achieved. We assume that if the microstrip radial stub is used to suppress the harmonics, the 3rd and 2nd harmonic frequencies can be still be suppressed even the suppressed frequencies may be shifted after fabrication. In order to achieve a first-pass design for the LTE inverse class F PA with 10 MHz bandwidth, the microstrip radial stub in (Wang *et al.*, 2012b) is used instead of using λ/4 straight stub to expand the suppression bandwidth at the 2nd and 3rd harmonic in case that the suppressed frequencies are shifted after fabrication. The input and output matching network structure with the microstrip radial stub as shown in Figure 101 is proposed. The procedure of designing the matching network is described as follows:

1. Analyze the microstrip radial stub structure alone before it being added in the matching network by Momentum simulation. Based on the analysis, chosen the angle and length of the microstrip radial stub.

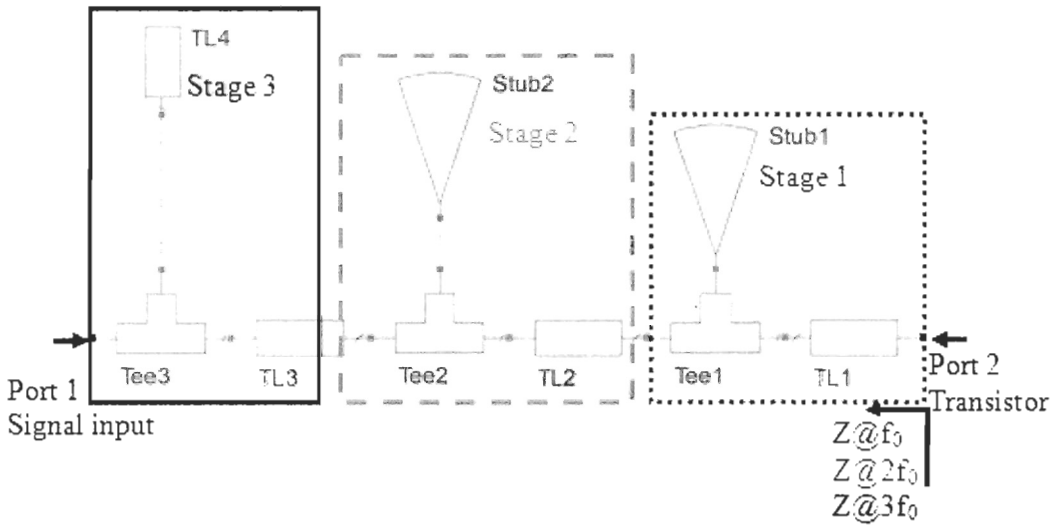
2. Determine the length of the microstrip radial stub Stub1 in stage 1 to suppress the 3rd harmonic frequency with 30 MHz bandwidth by Momentum simulation.

3. Determine the length of TL1 in stage 1 to achieve the target phase of the impedance at the 3rd harmonic frequency by Momentum simulation.

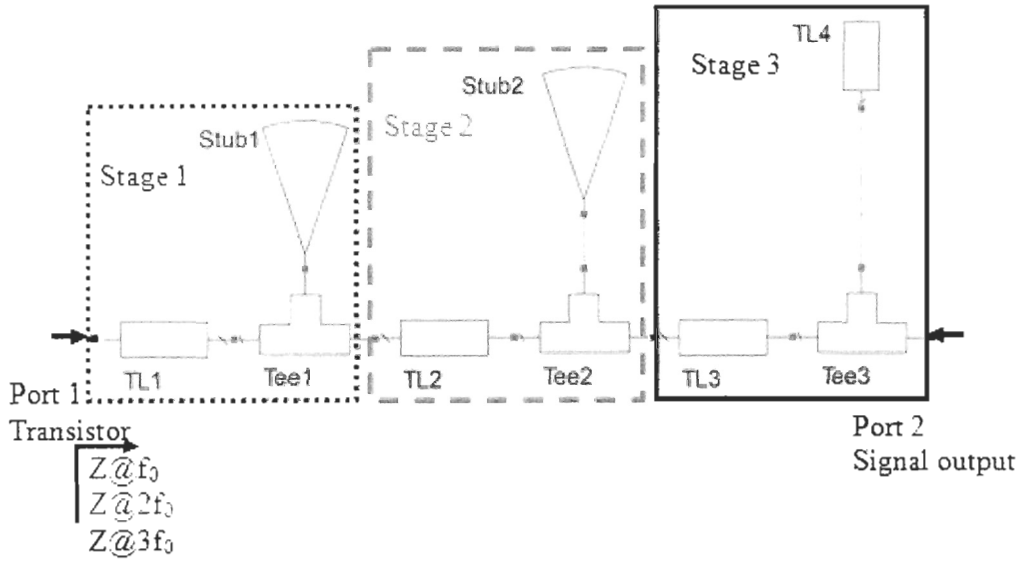
4. Determine the length of the microstrip radial stub Stub2 in stage 2 to suppress the 2nd harmonic frequency with 20 MHz bandwidth by Momentum simulation.

5. Determine the length of TL2 in stage 2 to achieve the target phase of the impedance at the 2nd harmonic frequency by Momentum simulation.

6. Determine the length of TL3 and TL4 in stage 3 to achieve the target impedance at the fundamental frequency by Momentum simulation.



(a)



(b)

Figure 101 : Proposed structure of input (a) and output (b) matching network with radial stub for the LTE inverse class F PA

5.6.1 Analyze of the microstrip radial stub

In this section, the microstrip radial stub is analyzed. The topology of the radial stub is shown in Figure 102, where θ is the angle of the radial stub, W is the bottom width of radial stub, and L is the length of radial stub. To analyze the suppression bandwidth of the radial stub at the 2nd and 3rd harmonic frequencies, θ *and* W are swept separately while L is optimized for obtaining the maximum suppression at the 2nd or 3rd harmonic frequency.

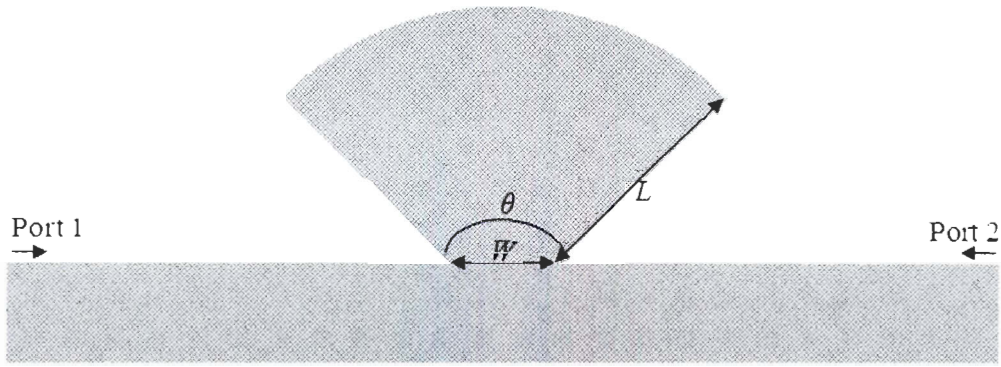


Figure 102 : Topology of the radial stub

For the radial stub which suppresses the 2nd harmonic frequency, Momentum simulation with 60 mesh is used to simulate the suppression of the radial stub. The used substrate is Rogers RT/duroid 5870 substrate with substrate thickness of 31 and 17 μm metal thickness. The width for 50 Ω line at 7 GHz is 91.34 mil, so W is swept from 131.34 mil to 51.34 mil with 20 mil step when θ is fixed to 90° and L is optimized for obtaining the maximum suppression at 7 GHz. From the result in Figure 103, we can see that larger W offers wider bandwidth of suppression. However, the insertion loss at 3.5 GHz is increased. By considering the suppression bandwidth of the harmonic frequency and the insertion loss at the fundamental frequency, W =91.34 mil is chosen for the radial stub to suppress the 2nd harmonic frequencies.

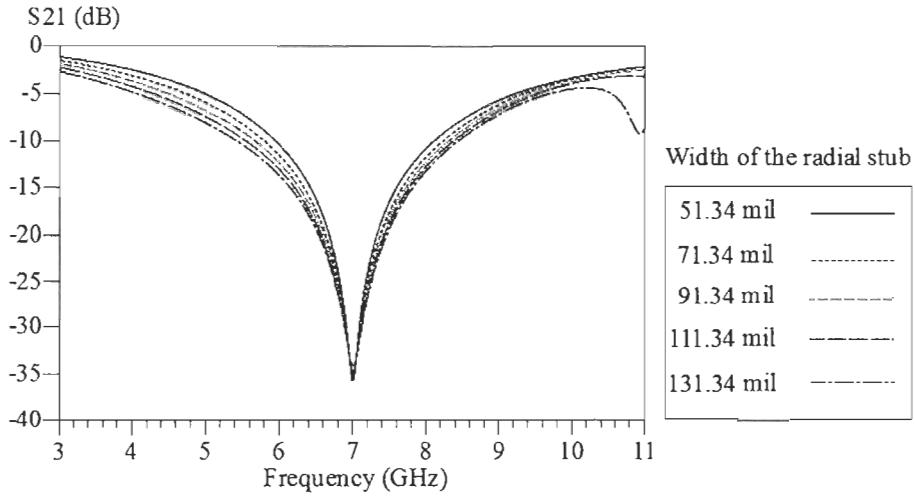


Figure 103 : Momentum results of the radial stub for 7 GHz when W is swept from 51.34 mil to 131.34 mil with θ=90°

To analyzer the effect of the angle of the radial stub, θ is swept from 10° to 170° while W is fixed to 91.34 mil and L is optimized for obtaining the maximum suppression at 7 GHz. From the Momentum result in Figure 104, we can see that larger angle of radial stub offers wider bandwidth of suppression, but the insertion loss at 3.5 GHz is increased.

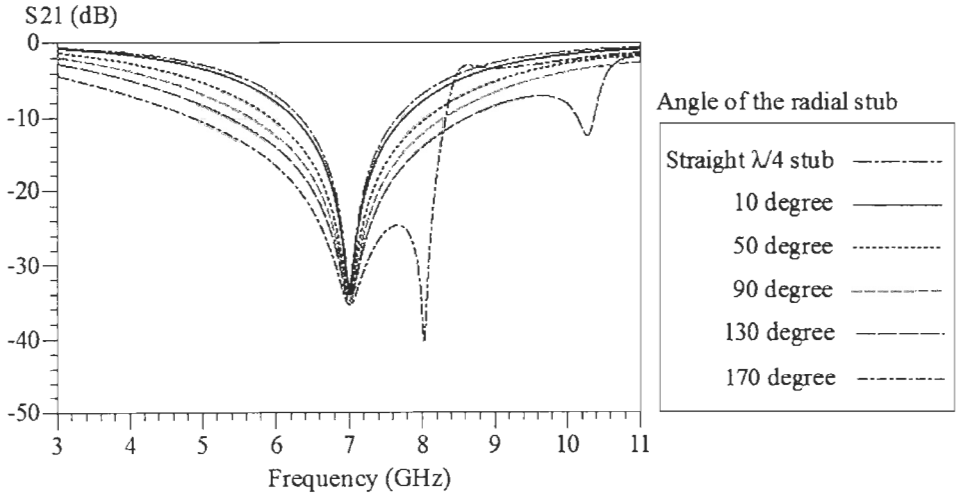


Figure 104 : Momentum results of radial stub for 7 GHz when θ is swept from 10° to 170° with W=91.34 mil

By considering the suppression bandwidth of the harmonic frequency and the insertion loss at the fundamental frequency, 90° is chosen for the radial stub to suppress the 2nd harmonic frequencies. With 91.34 mil of W, 90° of θ and 216.5 mil of L, the suppression at 7 GHz in 20 MHz bandwidth by the microstrip radial stub is between 34.62 to 34.70 dB.

For the radial stub which suppresses 3rd harmonic frequency, Momentum simulation with 60 mesh is used to simulate the suppression of the microstrip radial stub. The width for 50 Ω line at 10.5 GHz is 92.05 mil, so W is swept from 132.05 mil to 52.05 mil with 20 mil step when θ is fixed to 90° and L is optimized for obtaining the maximum suppression at 10.5 GHz. From the result in Figure 105, wider width of radial stub offers wider bandwidth of suppression. However, the insertion loss at 3.5 GHz is increased. By considering the suppression bandwidth of the harmonic frequency and the insertion loss at the fundamental frequency, W =92.05 mil is chosen for the radial stub.

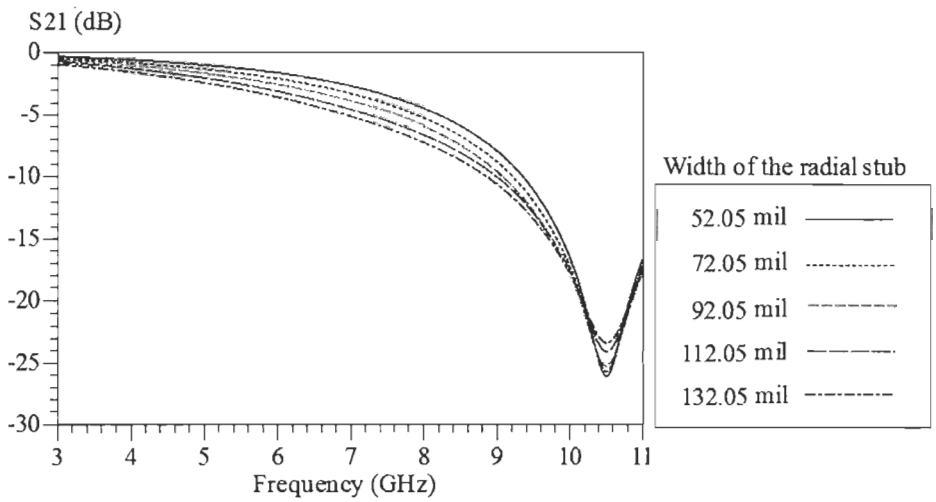


Figure 105 : Momentum results of radial stub for 10.5 GHz when W is swept from 132.05 mil to 52.05 mil with θ=90°

To analyzer the effect of the angle of the radial stub, θ is swept from 10° to 170° while W is fixed to 92.05 mil and L is optimized for obtaining the maximum suppression at

10.5 GHz as shown in Figure 106. From the Momentum result in Figure 106, we can see that larger angle of radial stub offers wider bandwidth of suppression, but the insertion loss at 3.5 GHz is increased.

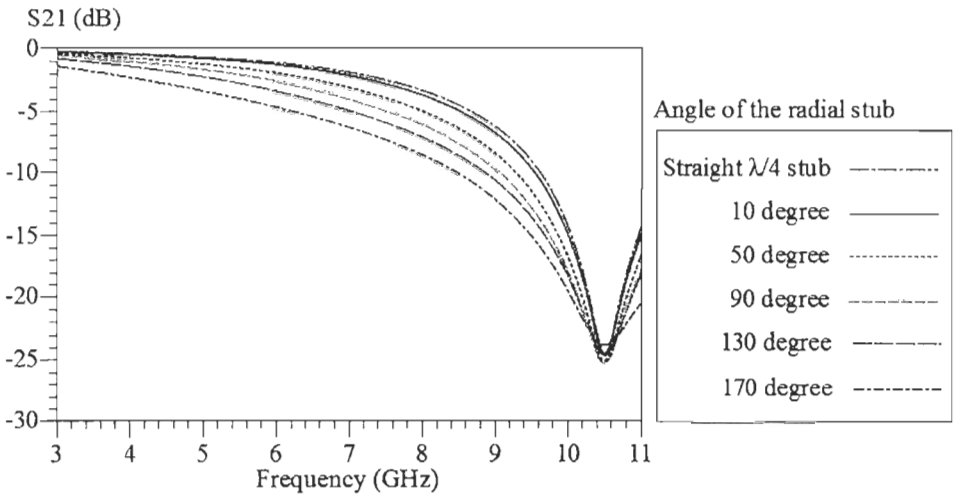


Figure 106 : Momentum results of radial stub for 10.5 GHz when θ is swept from 10° to 170° with W=92.05 mil

By considering the suppression bandwidth of the harmonic frequency and the insertion loss at the fundamental frequency, 90° is chosen for the radial stub to suppress 3rd harmonic frequencies. With 91.34 mil of W, 90° of θ and 141.8 mil of L, the suppression at 10.5 GHz in 30 MHz bandwidth by the microstrip radial stub is between 25.26 to 25.29 dB.

5.6.2 Design of the matching network for the LTE characterization result obtained by the multi-harmonic tuner system

With the microstrip radial stubs, the input and output matching network is designed by Momentum simulation with 60 mesh to match the impedances obtained in the LTE characterization in Table 19. The used substrate is Rogers RT/duroid 5870 substrate with 31 mil substrate thickness and 17 μm metal thickness.

To compare the bandwidth performance of radial stub matching network with the λ/4 straight stub matching network, the matching network with the λ/4 straight stub is also designed for matching the impedances obtained by the source & load pull tuner system with LTE signal in Table 19 in section 5.2. Momentum simulation results of the input and output impedance matching network with the radial stubs and Momentum simulation results of the input and output impedance matching network with the straight λ/4 stubs are compared in Figure 107 and Figure 108, respectively. The source and load impedances at 3.5 GHz, 7 GHz and 10.5 GHz achieved by the input and output matching network simulated by Momentum simulation with 60 mesh are compared with the target impedances in Table 33.

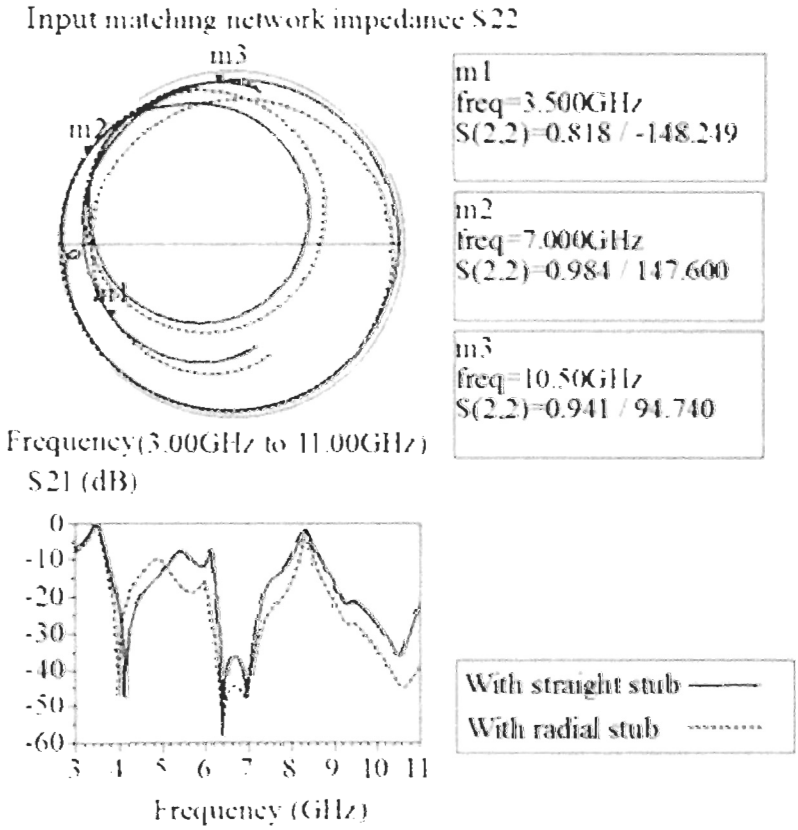


Figure 107 : Momentum simulation results of the input impedance matching network designed based on LTE characterization by the tuner system

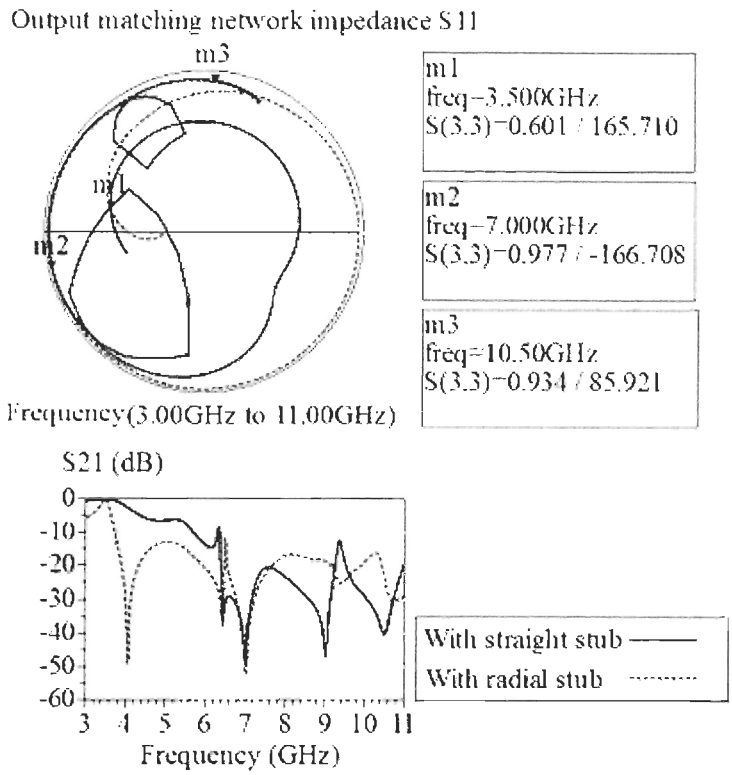


Figure 108 : Momentum simulation result of the output impedance matching network designed based on LTE characterization by the tuner system

Table 33 : Impedances chosen in the LTE characterization by the tuner system and the simulated impedances of matching networks by Momentum simulation

	LTE characterization result by the source & load pull tuner	**Simulated impedances of matching networks by Momentum simulation**
Load imp. @ 3.5 GHz	0.603∠165.5°	0.601∠165.7°
Load imp. @ 7 GHz	0.923∠-166.6°	0.977∠-166.7°
Load imp. @ 10.5GHz	0.929∠86.1°	0.934∠85.9°
Source imp. @ 3.5 GHz	0.818∠-148.2°	0.818∠-148.2°
Source imp. @ 7 GHz	0.929∠147.5°	0.984∠147.6°
Source imp. @ 10.5GHz	0.919∠94.8°	0.941∠94.7°

In Figure 108 and Table 33, we can see that the impedances of input and output matching networks with radial stub and λ/4 straight stub at 3.5 GHz, 7 GHz and 10.5 GHz are well designed to match the impedances in Table 19.

For the input impedance matching network with the radial stub based on the LTE characterization result obtained by the source & load pull tuner, the insertion loss at 3.5 GHz with 10 MHz bandwidth is between 0.33 dB and 0.35 dB. The suppression at 7 GHz with 20 MHz is between 48.06 dB and 47.84 dB. The suppression at 10.5 GHz with 30 MHz is 43.66 dB and 44.21 dB. Compared with the matching network with λ/4 straight stub, the suppression bandwidth for the 2nd and 3rd harmonic is increased by the radial stub in input matching network. For the 2nd harmonic, the 30 dBc suppression bandwidth of this input matching network with λ/4 straight stub is 0.82 GHz, while with radial stub is 1.08 GHz. For the 3rd harmonic, the 30 dBc suppression bandwidth of this input matching network with λ/4 straight stub is 0.55 GHz, while with radial stub is more than 1.29 GHz.

For the output impedance matching network with radial stub based on the LTE characterization result obtained by the source & load pull tuner, the insertion loss at 3.5 GHz with 10 MHz bandwidth is between 0.28 dB and 0.3 dB. The suppression at 7 GHz with 20 MHz bandwidth is between 35.92 dB and 50.41 dB. The suppression at 10.5 with 30 MHz bandwidth is between 22.53 dB and 24.19 dB. Compared with the matching network with λ/4 straight stub, the radial stubs in the output matching network do not increase the suppression bandwidth for the 2nd and 3rd harmonic. For the 2nd harmonic, the 30 dB suppression bandwidth of this input matching network with λ/4 straight stub is 0.45 GHz. The 30 dBc suppression bandwidth of this input matching network with radial stub is 0.43 GHz. For the 3rd harmonic, the 30 dB suppression bandwidth of this output matching network with λ/4 straight stub is 0.67 GHz. The 30 dBc suppression bandwidth of this output matching network with radial stub is only 0.21 GHz.

In this case, we can see that the radial stub cannot always increase the suppression bandwidth. Further research should be done to investigate this phenomenon. Therefore, the structure of output matching network with λ/4 straight stub at the 2nd and 3rd harmonic

frequencies in Figure 80 (b) in section 5.3 is chosen for the output matching network of the LTE inverse class F PA.

Table 34 summarized the dimensions of the components in the input and output matching network circuits designed based on the LTE characterization result obtained by the multi-harmonic source & load pull tuner system from Focus microwaves Inc.

Table 34 : The dimensions of the components in the input and output matching network circuits designed based on the LTE characterization result obtained by the tuner system

	Dimension	**TL1**	**Stub 1**	**TL2**	**Stub 2**	**TL3**	**TL4**	**Tee1**	**Tee2**	**Tee3**
Input matching network	**Length (mil)**	30.50	135.20	490.50	218.30	139.50	513.80	92.05	91.34	91.02
	Width (mil)	91.02	92.05 (50 Ω @ $3f_0$)	91.02	91.34 (50 Ω @ $2f_0$)	91.02	91.02 (50 Ω @ f_0)	91.02	91.02	91.02
	Dimension	**TL1**	**TL2**	**TL3**	**TL4**	**TL5**	**TL6**	**Tee1**	**Tee2**	**Tee3**
Output matching network	**Length (mil)**	62.10	185.30	183.50	285.00	720.20	221.00	92.05	91.34	91.02
	Width (mil)	91.02	92.05 (50 Ω @ $3f_0$)	91.02	91.34 (50 Ω @ $2f_0$)	91.02	91.02 (50 Ω @ f_0)	91.02	91.02	91.02

Figure 109 shows the layout of the input and output impedance matching network circuits designed for the matching the impedances obtained in the LTE characterization by the multi-harmonic source & load pull tuner system.

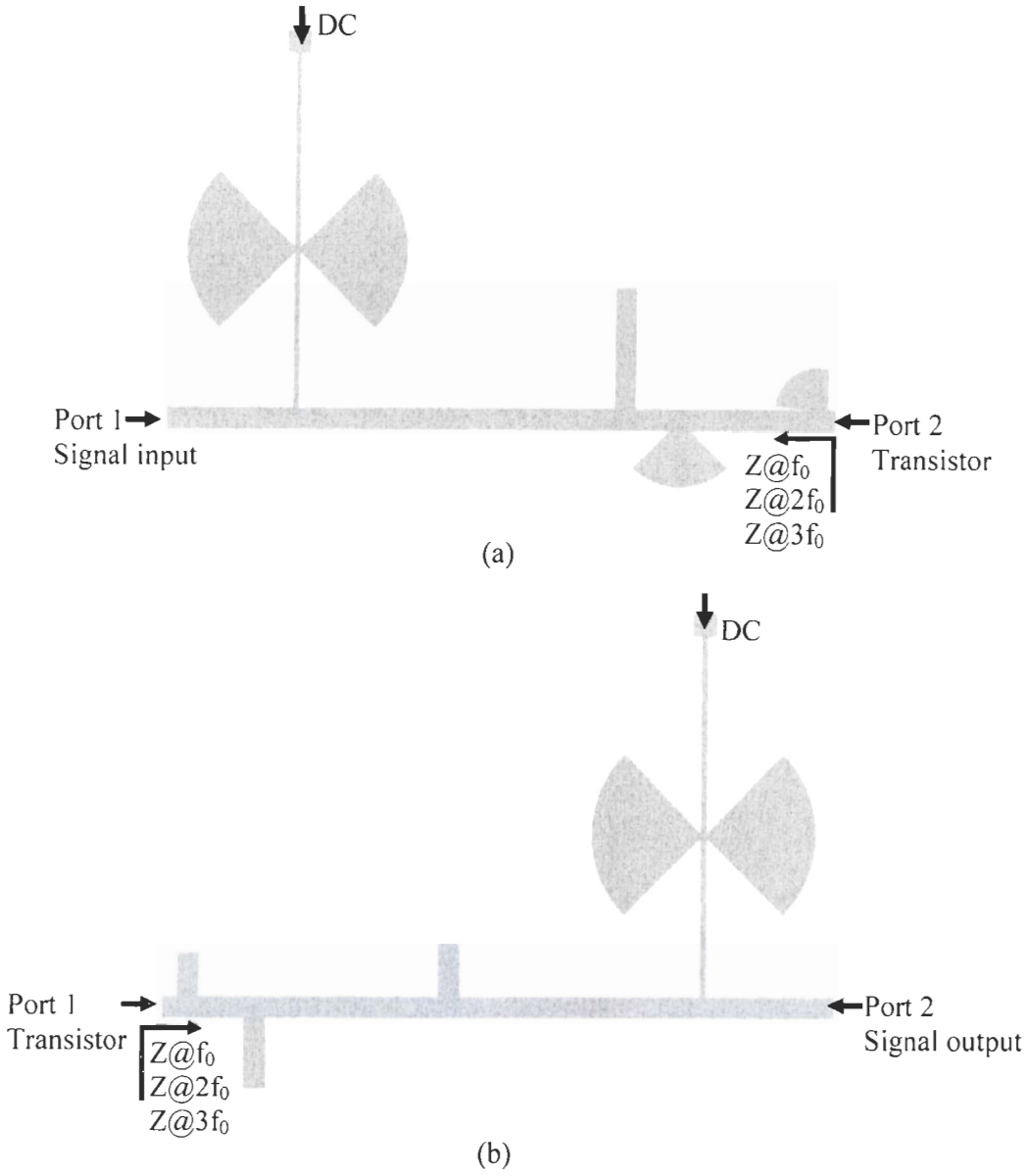


Figure 109 : Layout of the input (a) and output (b) matching network circuits designed based on the LTE characterization result obtained by the tuner system, where f_0 is 3.5 GHz

5.7 EVALUATION OF THE LTE CHARACTERIZATION RESULTS OBTAINED BY THE MULTI-HARMONIC TUNER SYSTEM

To evaluate the LTE characterization result obtained by the multi-harmonic tuner system in chapter 2, the LTE inverse class F PA is fabricated as shown in Figure 110. The LTE inverse class F PA is implemented on Rogers RT/duroid 5870 substrate with 31 mil substrate thickness and 17 μm metal thickness. In this LTE inverse class F PA circuit, 2 ATC 100B capacitors of 51 pF capacitance is used as the blocking capacitor. A Panasonic's 33 μF aluminum capacitor is used in the bias circuit as the bypass capacitor.

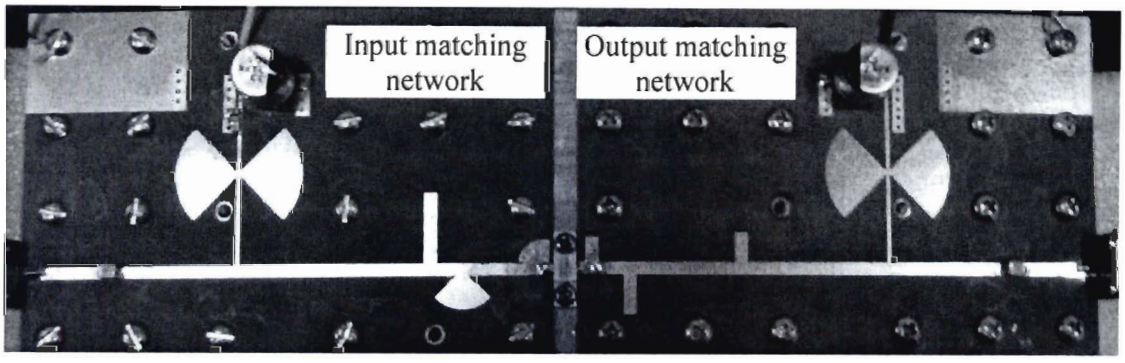


Figure 110 : Fabricated LTE inverse class F PA

The measured impedances and insertion loss of the input and output matching network are compared with simulation results obtained by Momentum simulation with 60 mesh in Figure 111. For the input impedance matching network designed based on the LTE characterization by the tuner system, the measured insertion loss at 3.5 GHz with 10 MHz bandwidth is between 1.42 dB and 1.65 dB. The suppression at 7 GHz with 20 MHz bandwidth is between 47.60 dB and 48.17 dB. The suppression at 10.5 GHz with 30 MHz bandwidth is between 30.14 dB and 31.18 dB. For the output impedance matching network designed based on the LTE characterization by the tuner system, the measured insertion loss at 3.5 GHz with 10 MHz bandwidth is between 0.19 dB and 0.82 dB. The suppression at 7 GHz with 20 MHz bandwidth is between 36.40 dB and 37.05 dB. The suppression at 10.5 GHz with 30 MHz bandwidth is between 30.10 dB and 30.96 dB.

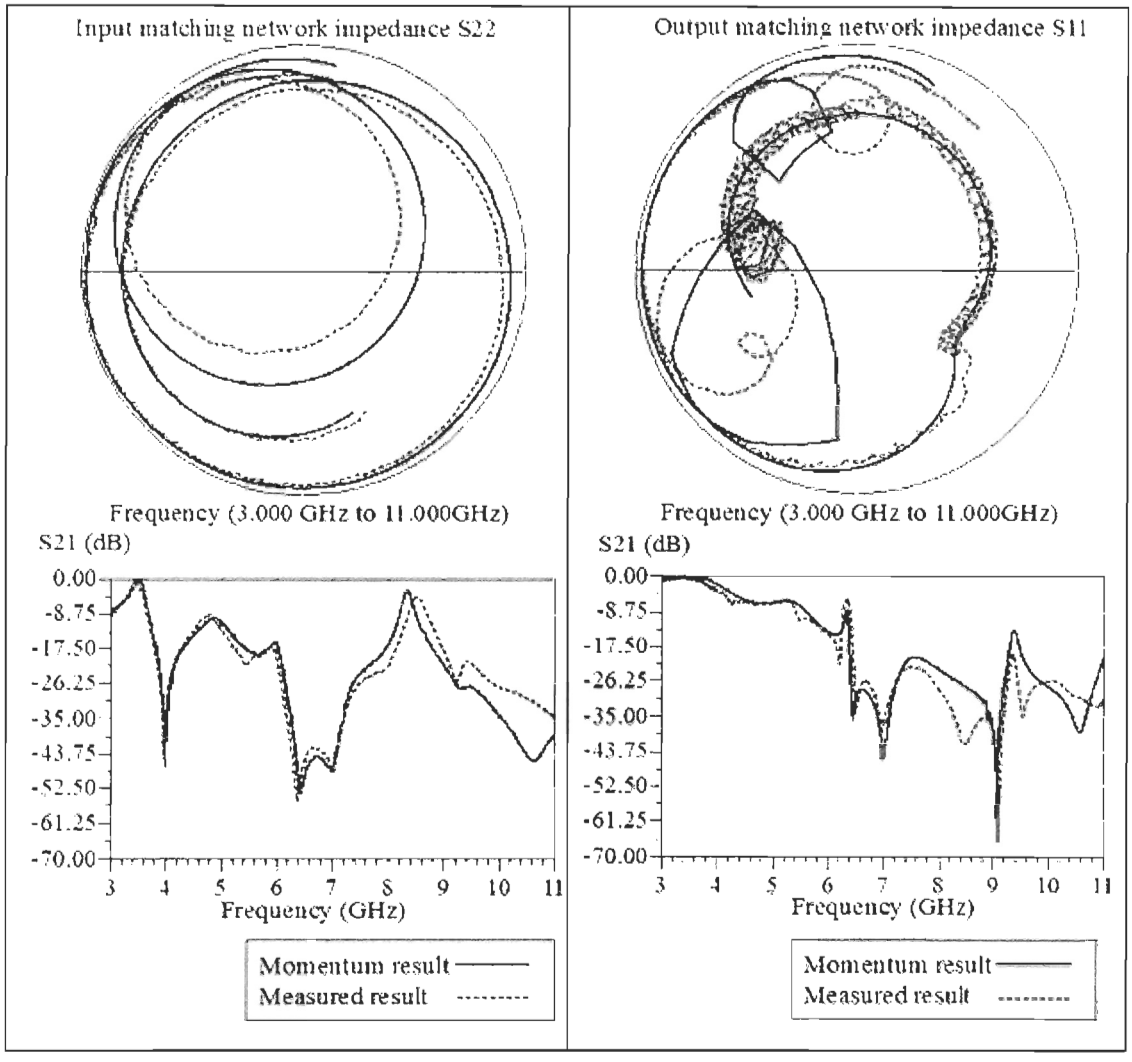


Figure 111 : Comparison of the measured and simulated impedances and insertion loss of the input (a) and output (b) matching networks designed based on the LTE characterization by the tuner system

The measured impedances and S_{21} of the matching network circuits are compared with the simulation results obtained by Momentum simulation with 60 mesh in Table 35. By comparison, we can see that the tendencies of the measured impedances and insertion loss of input and output matching network are similar to the simulation results. The 2nd and 3rd harmonics are well suppressed by the input and output matching network. However, there are 18.6°, 2.1° and 26.7° phase differences between the measured and simulated

phase of the load impedance at 3.5 GHz, 7 GHz and 10.5 GHz. 9.6°, 14.7° and 1.5° phase differences are existed between the measured and simulated phase of the source impedance at 3.5 GHz, 7 GHz and 10.5 GHz. These errors may be caused by my design method or fabrication. Further research should be made to minimize these errors.

Table 35 : The measured and simulated results of impedances and S_{21} of the matching network circuits designed based on the LTE characterization by the tuner system

	Measured impedances of matching networks	**Simulated impedances of matching networks by Momentum simulation**	**Measured S_{21} (dB)**	**Simulated S_{21} by Momentum simulation (dB)**
Load imp. @ 3.5 GHz	0.622∠147.1°	0.601∠165.7°	-0.55	-0.07
Load imp. @ 7 GHz	0.970∠-164.6°	0.977∠-166.7°	-36.81	-45.21
Load imp. @ 10.5GHz	0.841∠59.2°	0.934∠85.9°	-30.10	-37.63
Source imp. @ 3.5 GHz	0.810∠-157.8°	0.818∠-148.2°	-1.50	-0.34
Source imp. @ 7 GHz	0.947∠132.9°	0.984∠147.6°	-48.17	-47.93
Source imp. @ 10.5GHz	0.876∠93.20°	0.941∠94.7°	-30.14	-44.32

The LTE inverse class F PA designed based on the LTE characterization by the source & load pull tuner system is measured with LTE signal at 3.5 GHz with 10 MHz bandwidth by using the setup in Figure 91. A Rohde & Schwarz SMBV100A vector signal generator is used to generate the same input LTE signal at 3.5 GHz as the signal used in the LTE characterization. A N6705B DC power analyzer is used to provide DC power. An Agilent MXA signal analyzer with N9082A LTE TDD measurement application is used to measure the output power, ACPR 1 and ACPR 2 of the fabricated inverse class F PA. An Aeroflex Weinschel 40-30-34 attenuator is added at the output of the fabricated LTE inverse class F PA. The measured attenuation of this attenuator for the 10 MHz bandwidth LTE signal at 3.5 GHz is 31.7 dB.

With the measurement setup mentioned above, the fabricated LTE inverse class F PA is measured with 10 MHz bandwidth LTE signal at 3.5 GHz, when it is biased at V_{GS}=-2.58 V and V_{DS}=28 V. The measured PAE, gain, the worst ACPR 1 and ACPR 2 of this LTE inverse class F PA as a function of output power are shown in Figure 112.

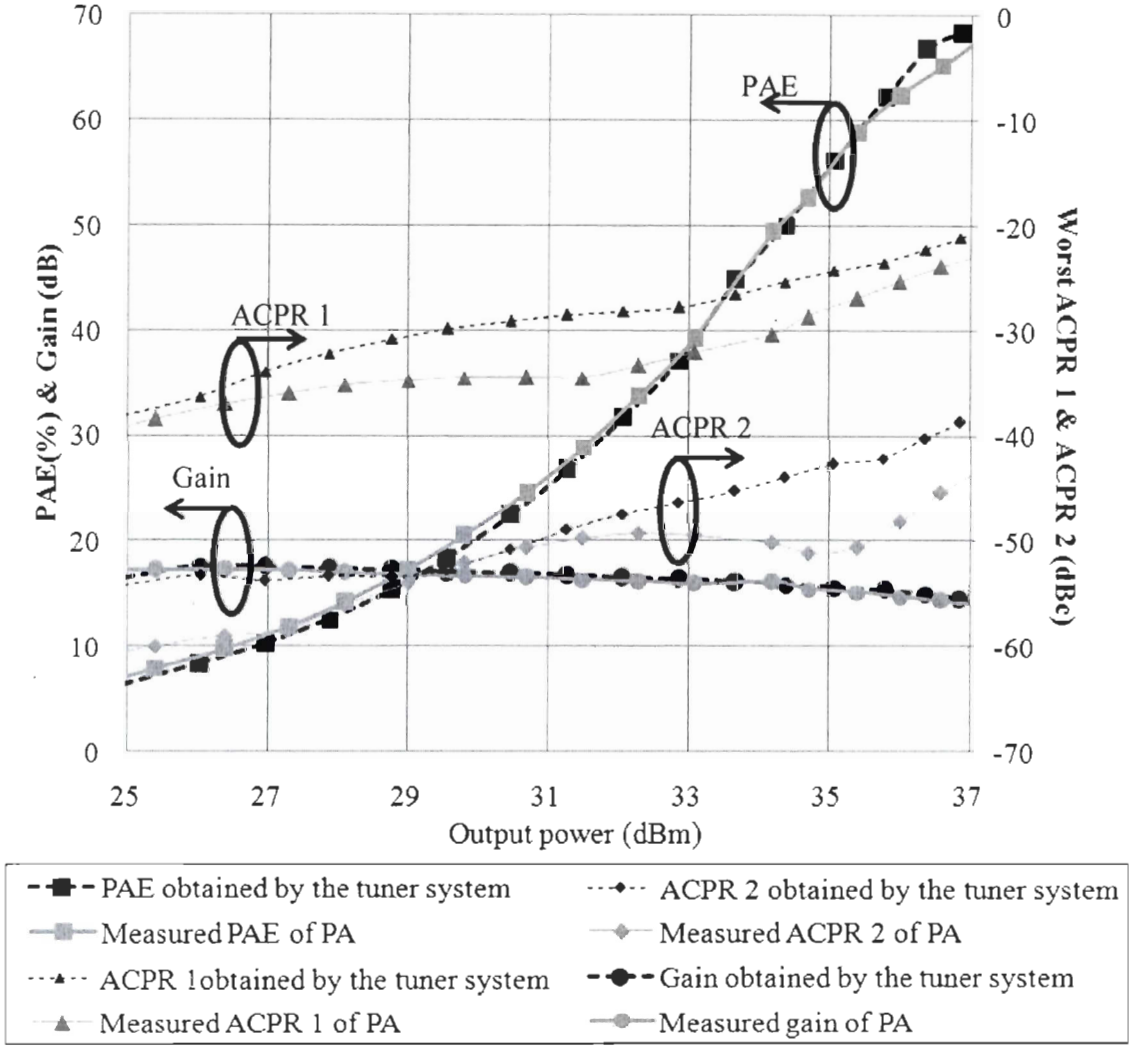


Figure 112 : Measured PAE, gain, worst ACPR 1 and ACPR 2 of the fabricated LTE inverse class F PA (gray) and the measured PAE, gain, ACPR 1 and ACPR 2 in the LTE characterization by the tuner system with 10 MHz bandwidth LTE signal at 3.5 GHz

When the input power of LTE signal is 18.00 dBm (input LTE signal spectrum is shown in Figure 113), the measured output power of the fabricated inverse class F PA can reach 34.20 dBm with 49.56% PAE. The worst ACPR 1 and ACPR 2 are -29.45 dBc and -50.87 dBc, respectively. The output LTE signal spectrum is shown in Figure 114. The maximum PAE 69.78% is found when the output power is 38.10 dBm and the gain is 13.30 dB with the worst ACPR 1/ACPR 2 of -20.50/-39.10 dBc. Based on the LTE characterization result obtained by the source & load pull tuner system in chapter 2, when the input power is 18.00 dBm, 51.48% PAE with 34.24 dBm output power, -24.23 dBc worst ACPR 1 and -42.40 dBc worst ACPR 2 are expected. In Table 36, the measured results of the fabricated inverse class F PA and the LTE characterization results obtained by the tuner system are compared.

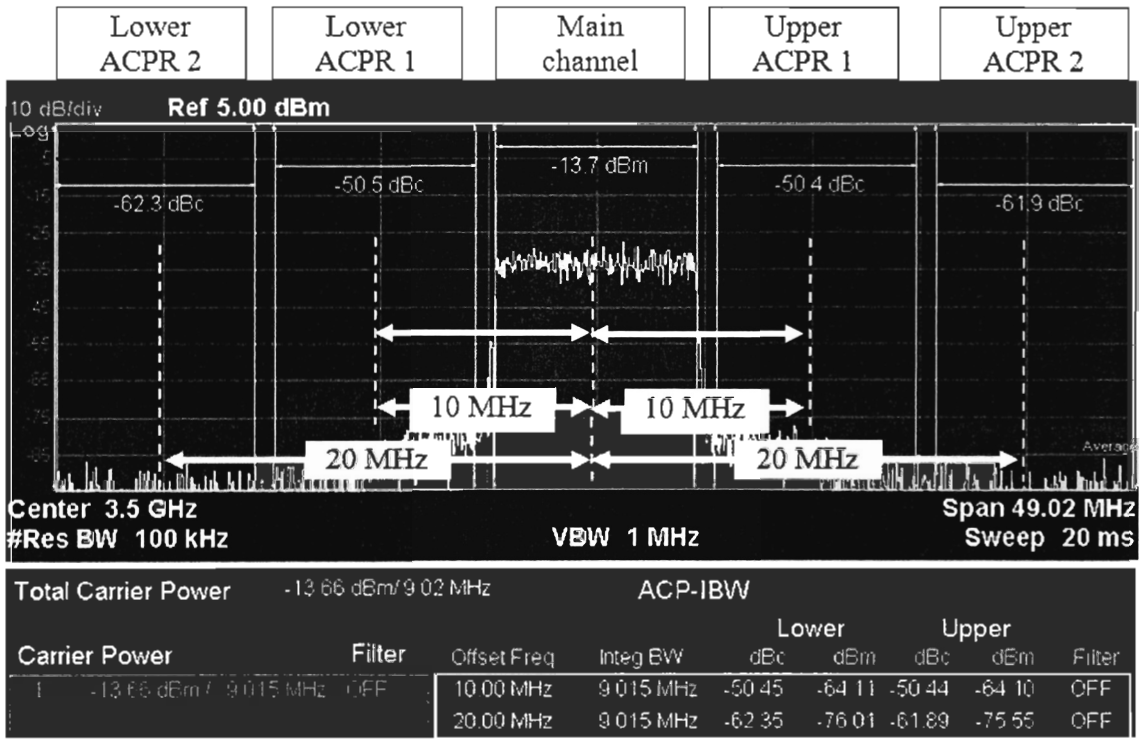


Figure 113 : Spectrum of the 18 dBm input LTE signal (after 31.7 dB attenuation)

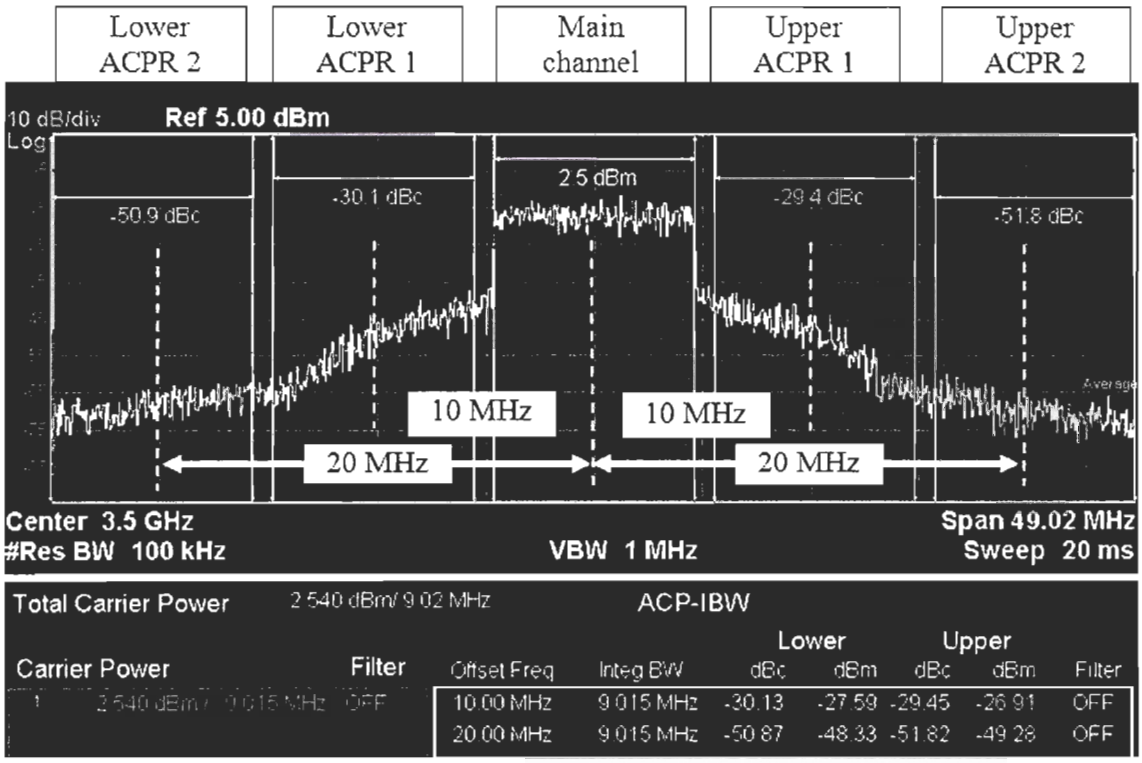


Figure 114 : Spectrum of the output LTE signal (after 31.7 dB attenuation)

Table 36 : Measured results of the fabricated LTE inverse class F PA and the LTE characterization results obtained by the tuner system

	Measured results of fabricated LTE inverse class F PA	**LTE characterization results obtained by tuner system**
PAE (%)	49.56	51.48
Pout (dBm)	34.20	34.24
Gain (dB)	16.20	16.24
Lower ACPR 1/Upper ACPR 1 (dBc)	-30.13/-29.45	-26.23/-24.23
Lower ACPR 2/Upper ACPR 2 (dBc)	-50.87/-51.82	-44.64/-42.40

From Table 36, we can see that the measured PAE is 1.92% less than the PAE obtained in characterization and measured output power is 0.04 dBm less than the output power obtained in the characterization. However, the ACPR 1 and ACPR 2 are lower than the results in the characterization. These differences in the results may be caused by the differences between the impedances achieved by the fabricated matching network and the impedances obtained in the characterization. Further research should be operated to minimize the differences between the measured results and the characterization results.

Table 37 summarizes the measured results of the PAs with the CGH40010 transistor for the modulated signals in another authors' works without linearization. From Table 37, we can see that the LTE inverse class F PA in this work provides the highest PAE when the worst ACPR 1 and ACPR 2 are less than -24 dBc.

Table 37 : Published works of PA with CGH40010 transistor with modulated signals

References	**Signal**	**Frequency (GHz)**	**PAE (%)**	**P_{out} (dBm)**	**Worst ACPR 1 (dBc)**	**Worst ACPR 2 (dBc)**
(Moon *et al.*, 2011)	LTE (10MHz bandwidth)	1.84	29.05	34.99	-25.14 (7.5 MHz offset)	-32.24 (12.5 MHz offset)
(Kim *et al.*, 2010c)	WiMAX (10MHz bandwidth)	2.56	55.80	36.00	-17.40 (5.3 MHz offset)	N/A
(Wang *et al.*, 2011)	OFDM (20MHz bandwidth)	2.55	31.30	33.60	-35.40 (N/A)	N/A
This work	LTE (10MHz bandwidth)	3.50	49.56	34.20	-29.45 (10 MHz offset)	-50.87 (20 MHz offset)

5.8 CONCLUSION

In this chapter, for evaluating the characterization results obtained by the multi-harmonic tuner system and by the simulation in chapter 2, the 1-tone and LTE inverse class F PAs are designed based on the characterization results in chapter 2. The measured results

of the 1-tone inverse class F PAs are compared with the 1-tone characterization results in chapter 2. Based on the comparison, we found that the multi-harmonic source & load pull tuner predicts the PAE and output power more precisely than the source & load pull simulation with large signal model as we expected. Thus, the multi-harmonic source & load pull tuner is recommended to be used for a first-pass design methodology for designing an inverse class F PA.

At 3.5 GHz, the 1-tone inverse class F PA designed based on the results obtained by the source & load pull tuner system offers the a PAE of 79.76% when output power is 40.02 dBm and the gain is 12.08 dB. Compared with other published works for inverse class F PAs, this inverse class F PA achieves the highest PAE at 3.5 GHz.

For the LTE inverse class F PA, the microstrip radial stub is analyzed and used in the matching network to achieve a first-pass design. The measured results of the fabricated LTE inverse class F PA shows that when this PA is under an excitation of a LTE signal at 3.5 GHz with 10 MHz bandwidth, it offers an output power of 34.20 dBm with a PAE of 49.56% and a gain of 16.20 dB when the worst ACPR1 and ACPR 2 are -29.45 dBc and -50.87 dBc, respectively. Compared with other published works for LTE PAs, the LTE inverse class F PA in this work provides the highest PAE when the ACPR 1 and ACPR 2 are less than -24 dBc.

Our contribution in this work is that we proved the multi-harmonic source & load pull tuner system can characterize the transistor more precisely than the simulation with large signal model. With this characterization method by using multi-harmonic source & load pull tuner system, we can design the inverse class F PA without post-production tuning.

CHAPITRE 6
CONCLUSION GÉNÉRALE

Les APs de haute efficacité ne sont pas encore fabriqués en large quantité en raison de l'absence de la méthodologie de conception qui nous permet d'avoir de bons résultats lors de la première fabrication. La méthodologie de conception de premier passage pourrait aider l'industrie à fabriquer des APs de haute efficacité en large quantité sans le réglage de postproduction. Dans ce mémoire, une méthodologie a été présentée pour la conception des APs de classe F inverse avec le signal 1-ton et le signal LTE. Pour commencer, le transistor CGH40010 est caractérisé et analysé par la simulation *source & load pull* dans ADS 2011.10 et par le système *source & load pull tuner* multi-harmonique passif de *Focus microwaves Inc.* Les $2^{ème}$ et $3^{ème}$ harmoniques à l'entrée et à la sortie du transistor sont pris en compte dans les caractérisations. À la connaissance de l'auteur, c'est la première fois que les $2^{ème}$ et $3^{ème}$ harmoniques à l'entrée du transistor sont pris en compte dans les caractérisations par le système *source & load pull tuner* multi-harmonique avec un signal 1-ton et un signal LTE. Selon l'analyse des résultats de la caractérisation par la simulation et le système *source & load pull tuner*, il a été prouvé que, en plus des $2^{ème}$ et $3^{ème}$ harmoniques à la sortie du transistor, les $2^{ème}$ et $3^{ème}$ harmoniques à l'entrée du transistor sont importantes pour un AP de classe F inverse pour atteindre un PAE élevé et une puissance de sortie élevée.

Les accessoires utilisés dans le système *source & load pull tuner*, tels que les tés de polarisation, les coupleurs directionnels et l'isolateur, sont analysés pour augmenter le coefficient de réflexion (Γ) maximal du système *source & load pull tuner*. Sur la base de cette analyse, le Γ maximal du *tuner* passif pourrait être augmenté de 0.902 à 0.930 par un bon choix des accessoires.

Sur la base des résultats de caractérisation obtenus par la simulation et le système *source & load pull tuner* multi-harmonique, les APs de classe F inverse pour le signal 1-ton et le signal LTE sont fabriqués et mesurés. En comparant la mesure des résultats des APs fabriqués sur la base des résultats de la caractérisation correspondants, nous avons constaté que le système *source & load pull tuner* multi-harmonique passif peut prédire les résultats, tels que le PAE et la puissance de sortie, plus précisément que la simulation de *source & load pull* dans ADS avec le modèle du transistor de grand signal. Ainsi, afin de réaliser une conception de premier passage pour les APs, le système *source & load pull tuner* est recommandé. De plus, par rapport aux recherches des autres auteurs traitant le transistor CGH40010, l'AP de classe F inverse conçu sur la base des résultats de caractérisation obtenus par le système *source & load pull tuner* avec le signal de 1-ton offre le PAE le plus élevé lorsque la puissance de sortie est supérieure à 40 dBm à 3.5 GHz. Lorsque la puissance de sortie est de 40.02 dBm, cet AP de classe F inverse pour le signal 1-ton offre 79.76% de PAE avec 12.08 dB de gain. Pour l'AP de classe F inverse conçu sur la base des résultats de caractérisation pour un signal LTE obtenu par le système de *tuner*, lorsque la mesure de la puissance de sortie est de 34.20 dBm avec 49.56% de PAE et 16.20 de gain, quand l'ACPR 1 est de -29.45 dBc et que l'ACPR 2 est de -50.87 dBc.

À l'avenir, le système *source & load pull tuner* multi-harmonique passif pourrait être utilisée pour caractériser les transistors d'autre entreprise, comme TriQuint Semiconductor Inc., ou pour des signaux plus avancés, comme signal de $5^{ème}$ Génération (5G).

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